

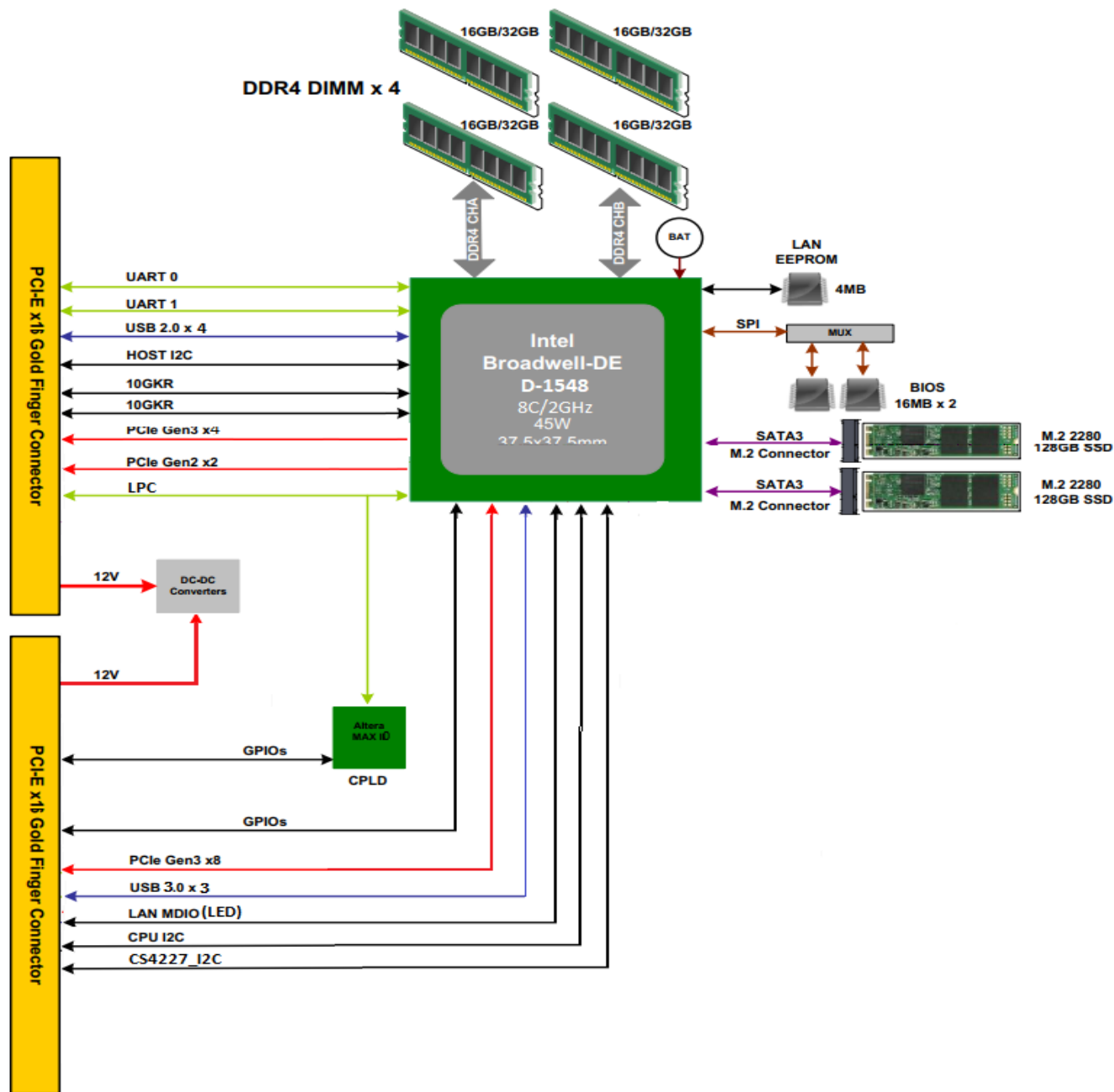
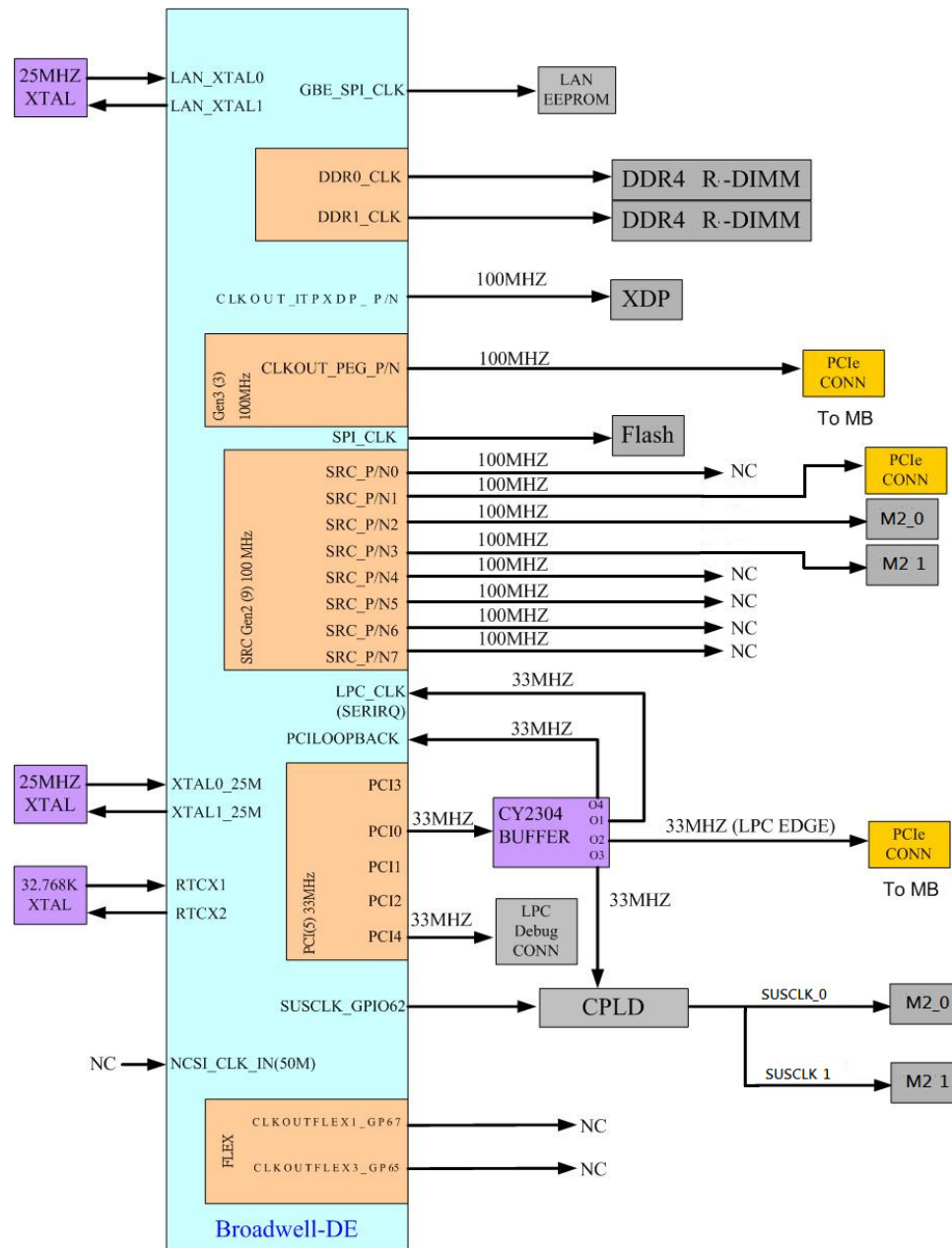
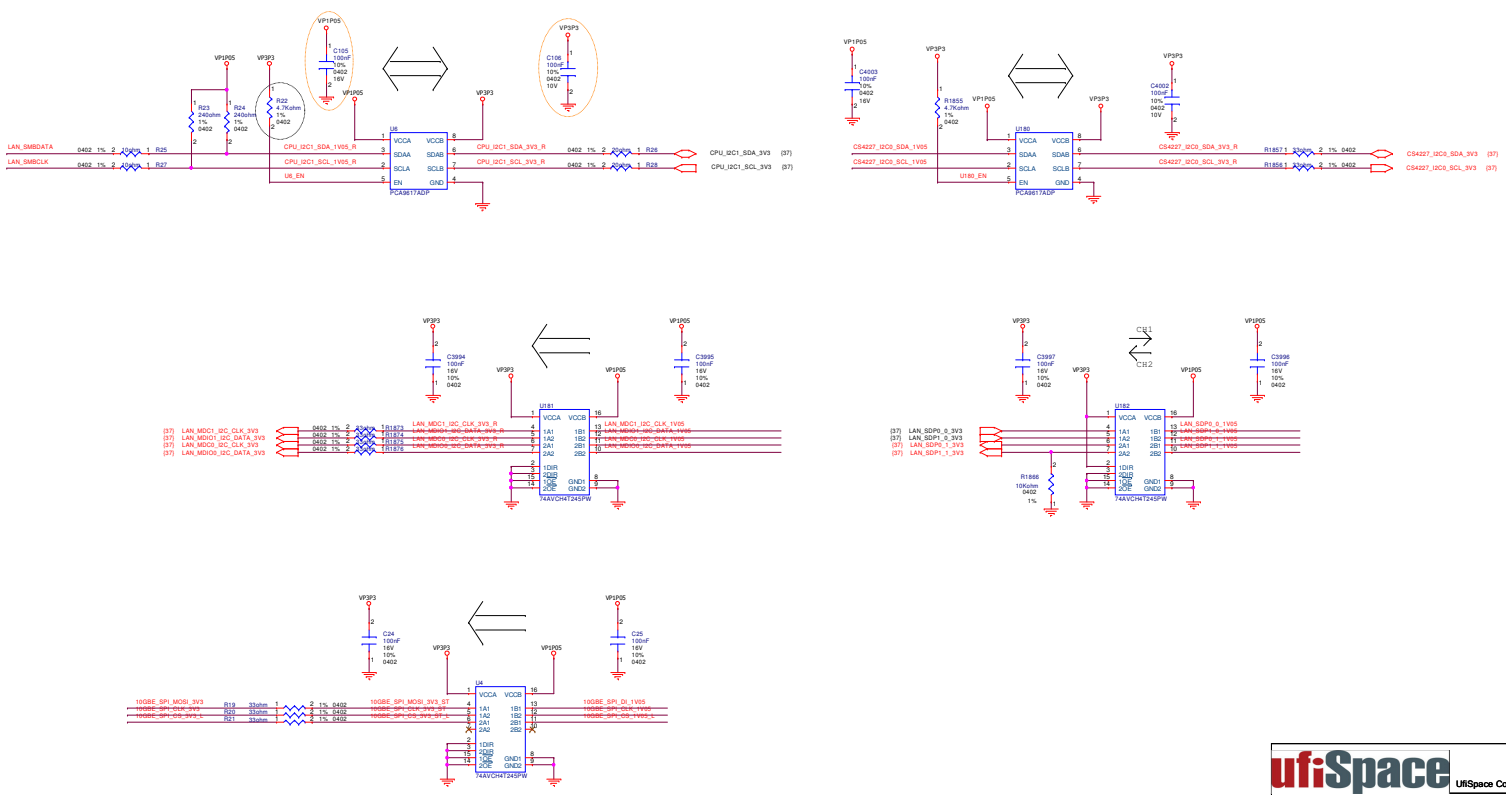
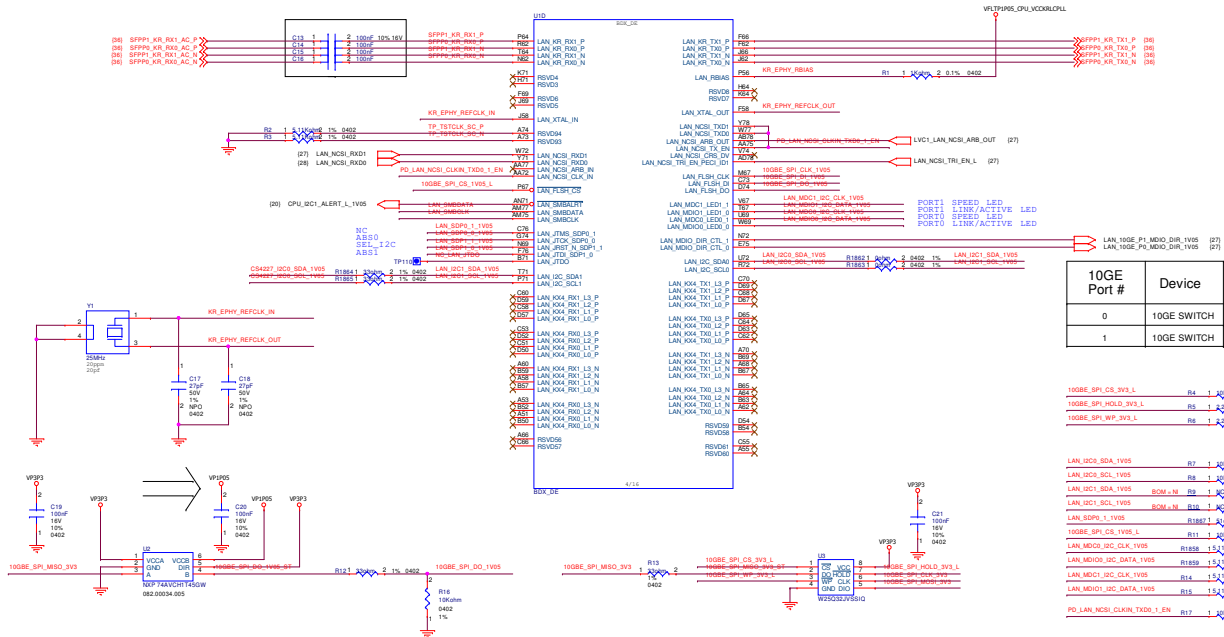
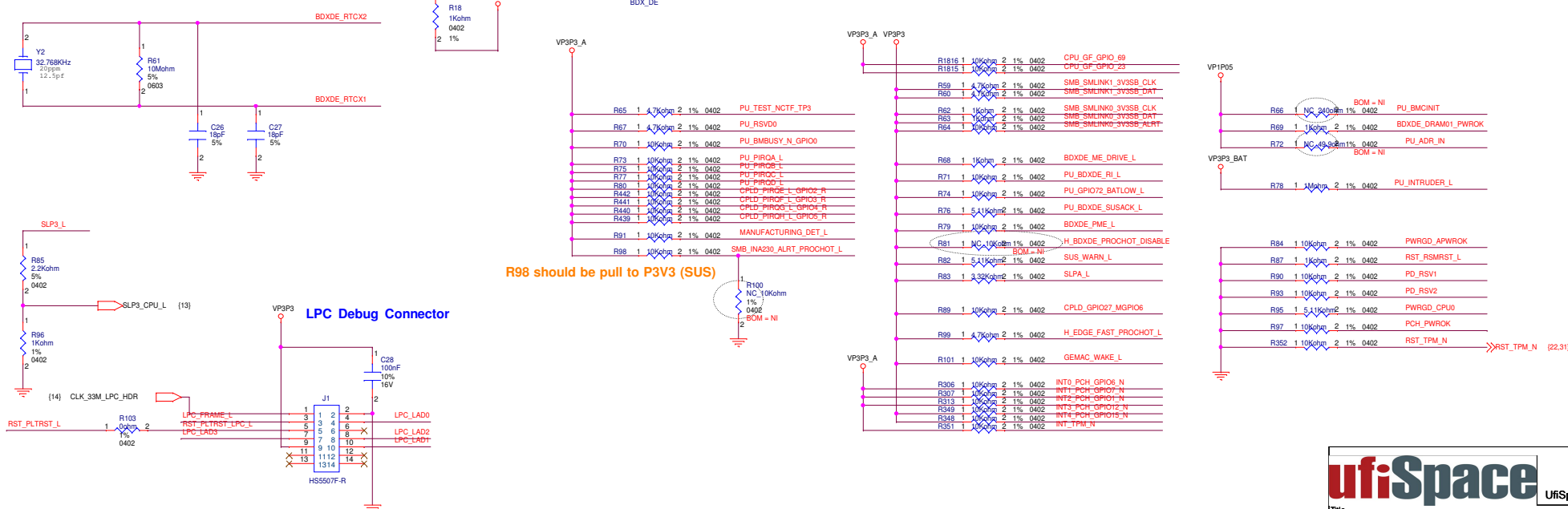
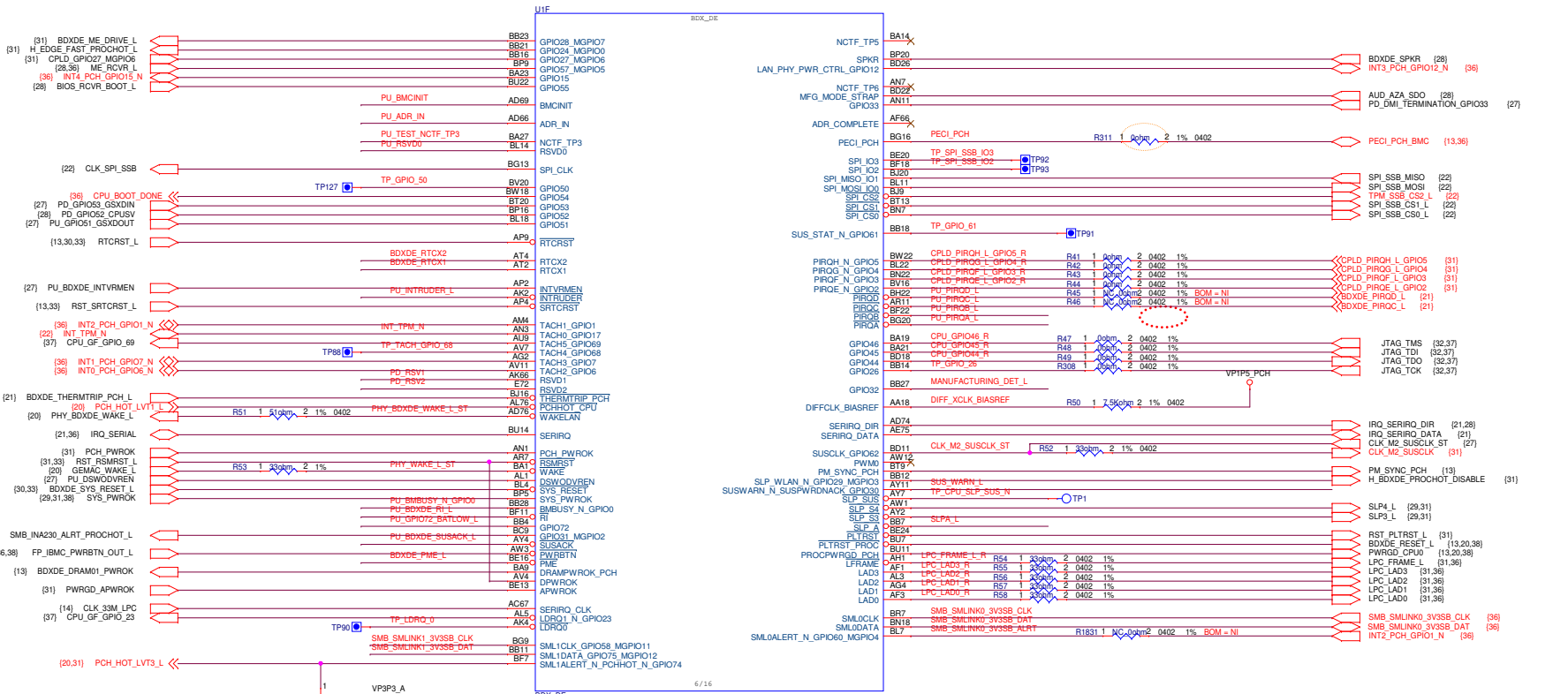


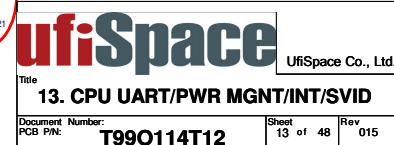
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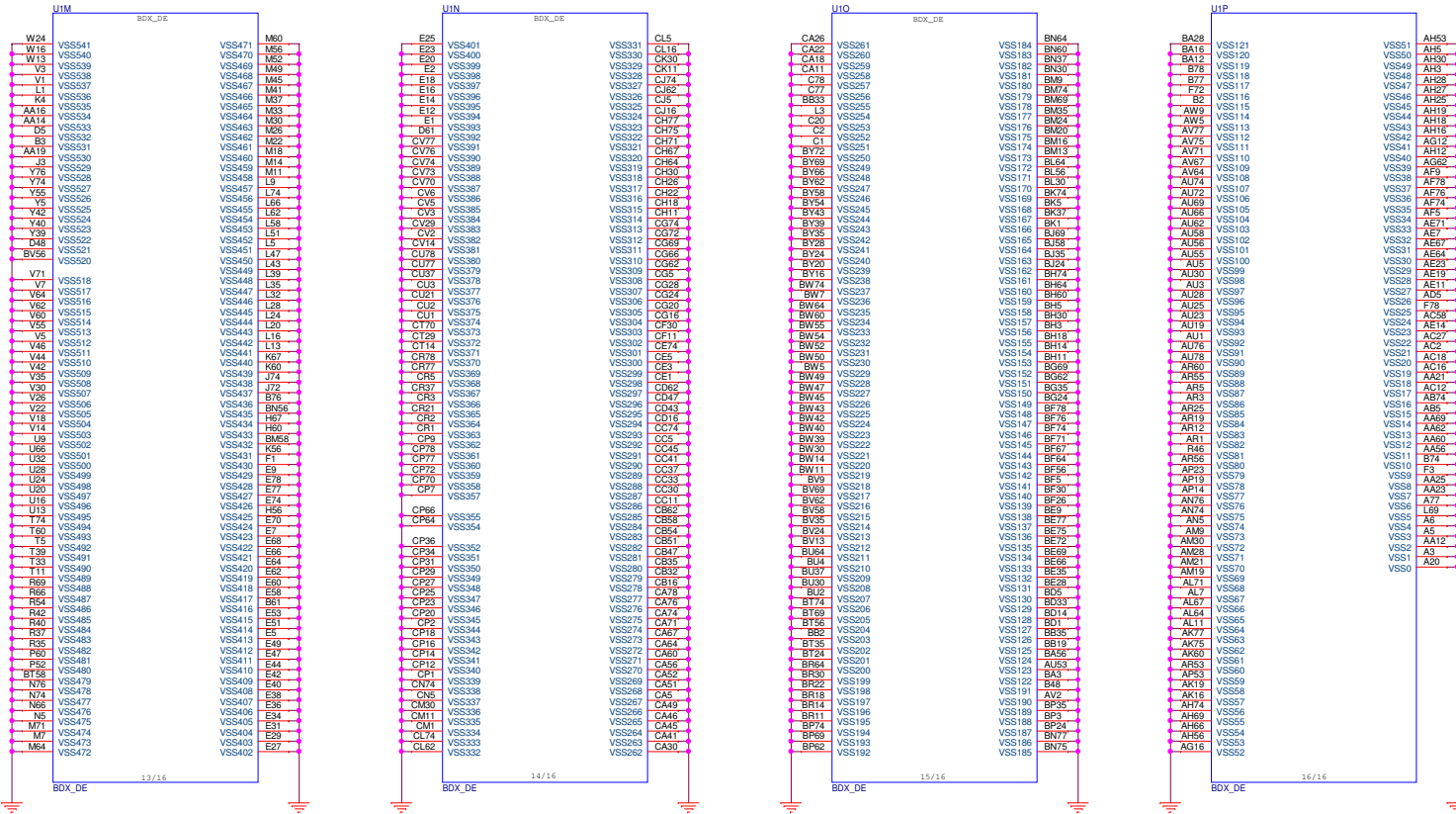
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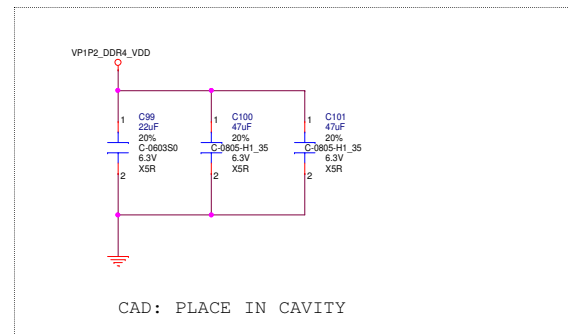
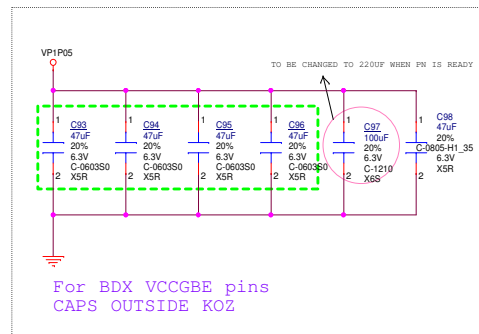
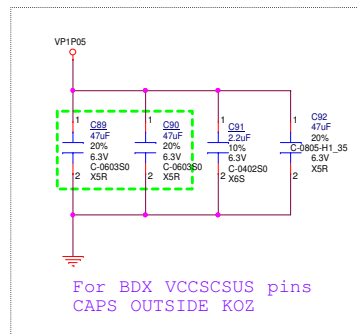
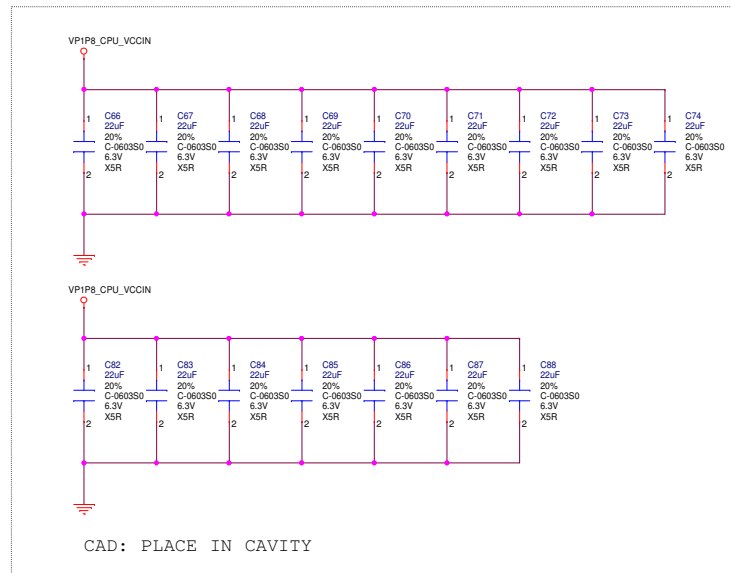
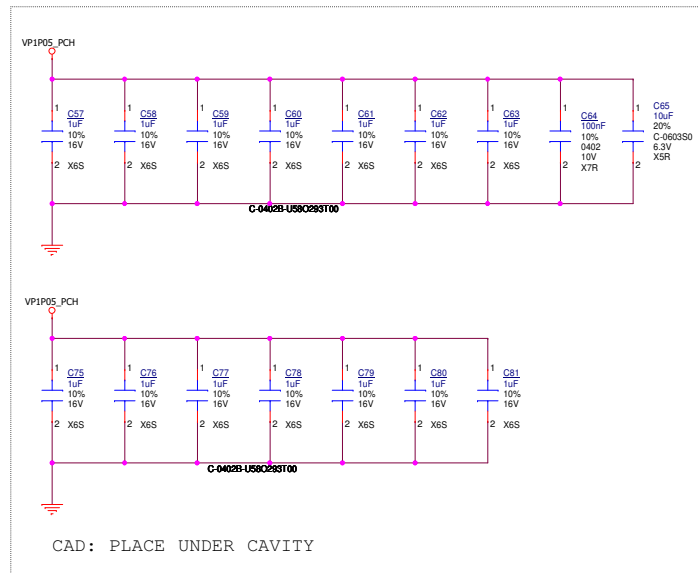
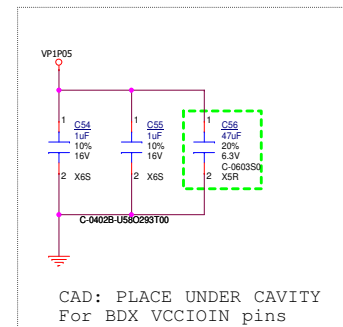
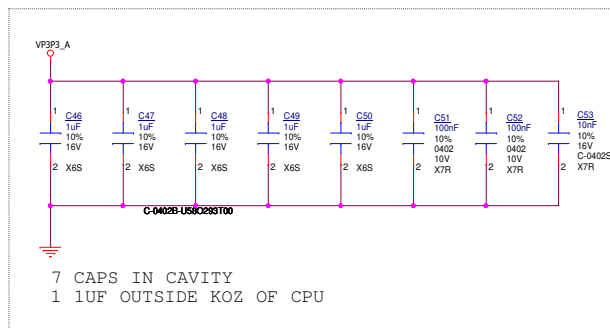
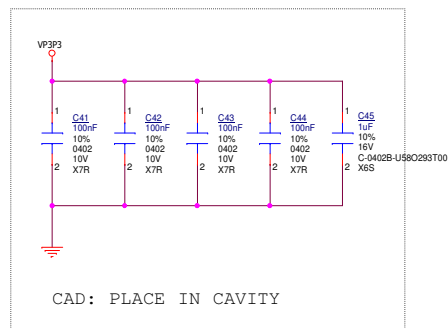


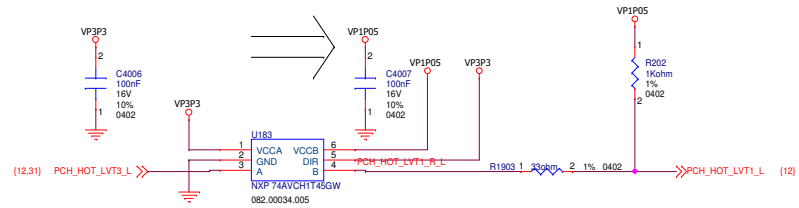
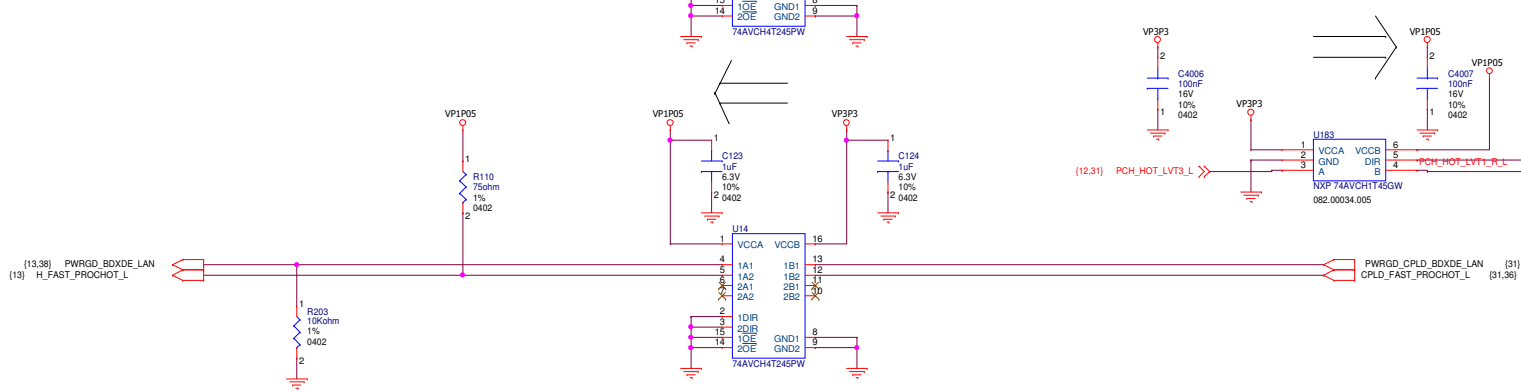
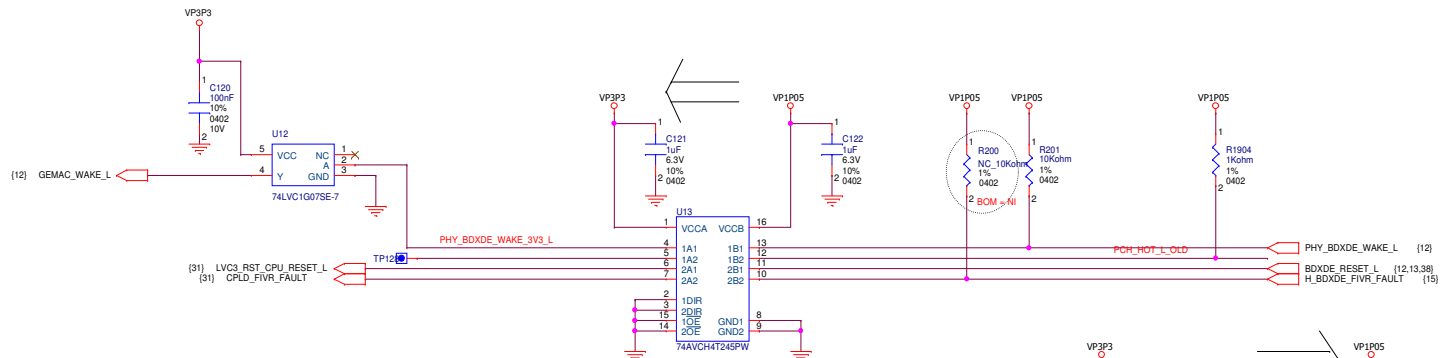
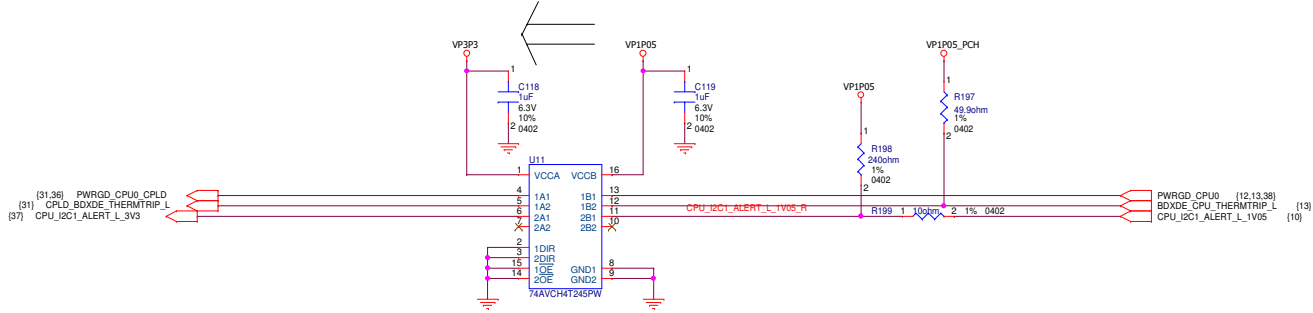
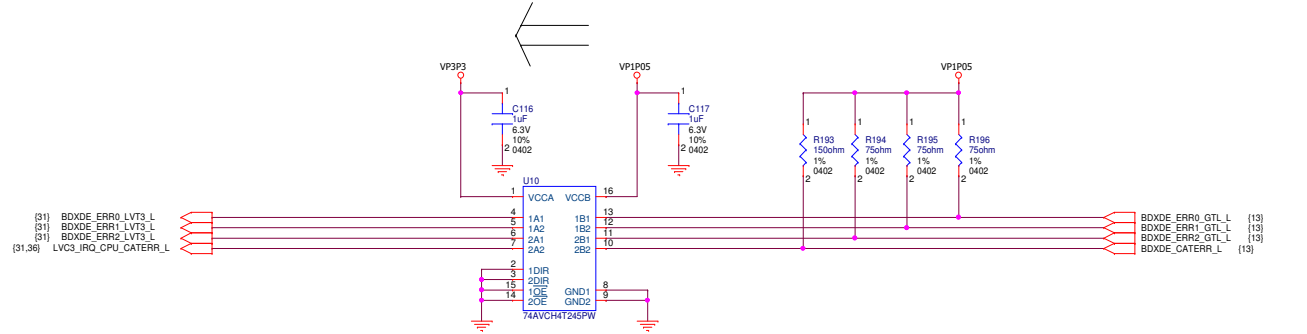


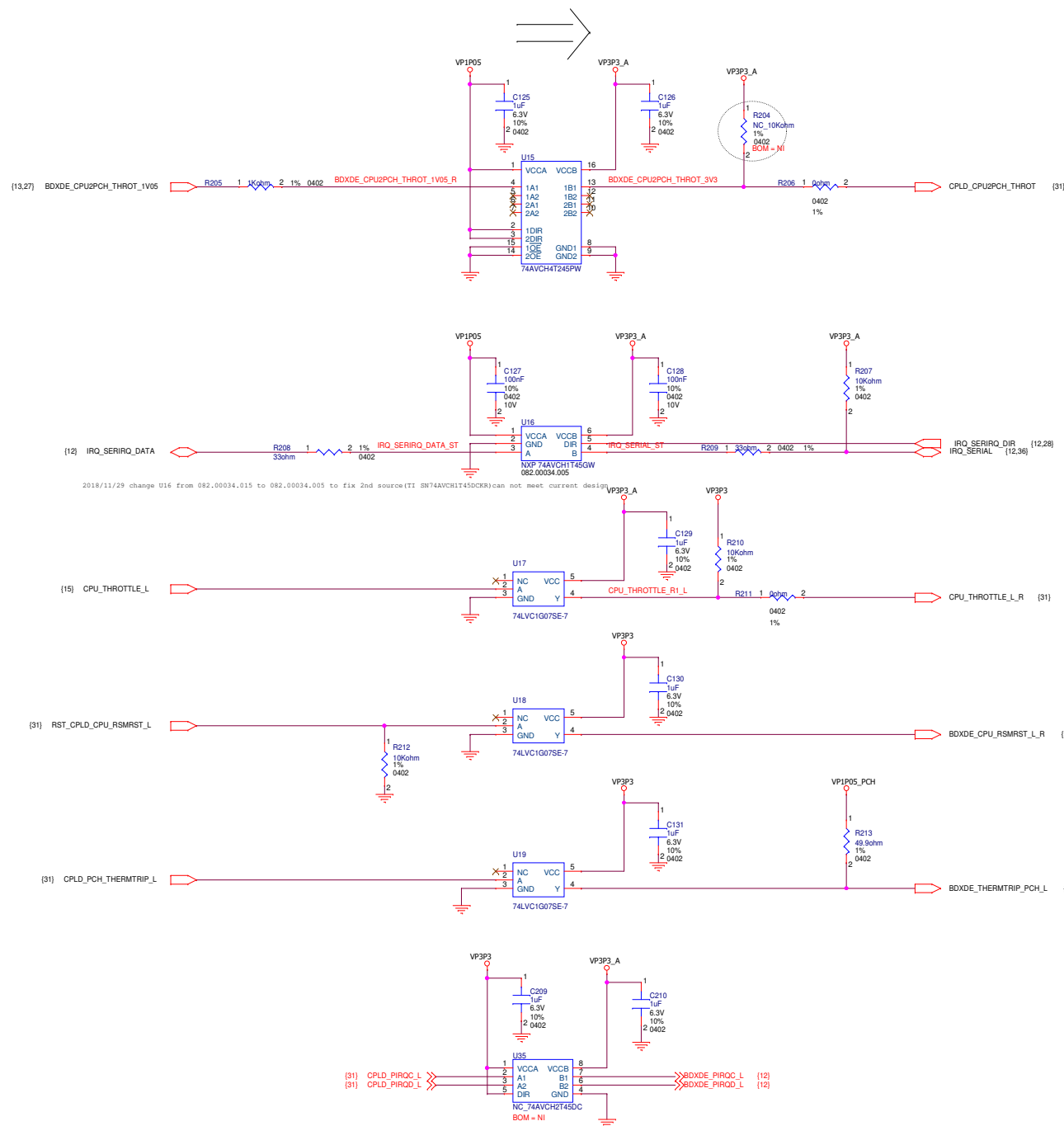


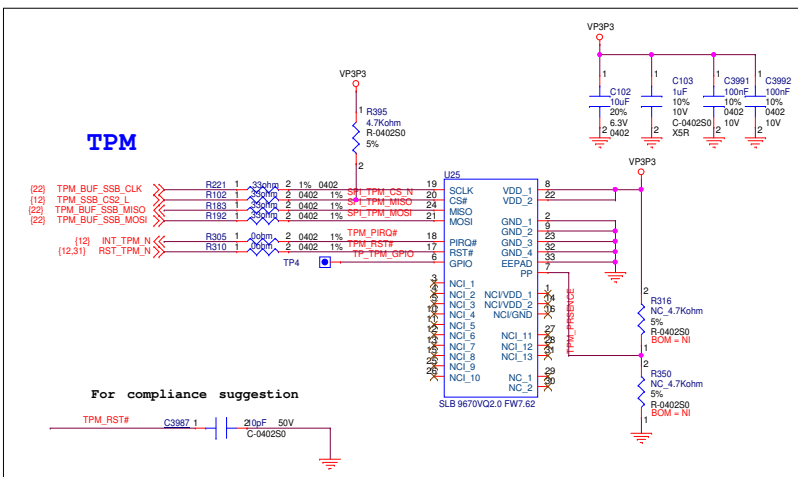
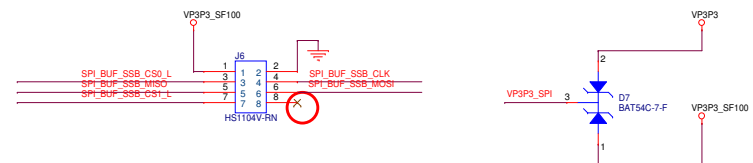




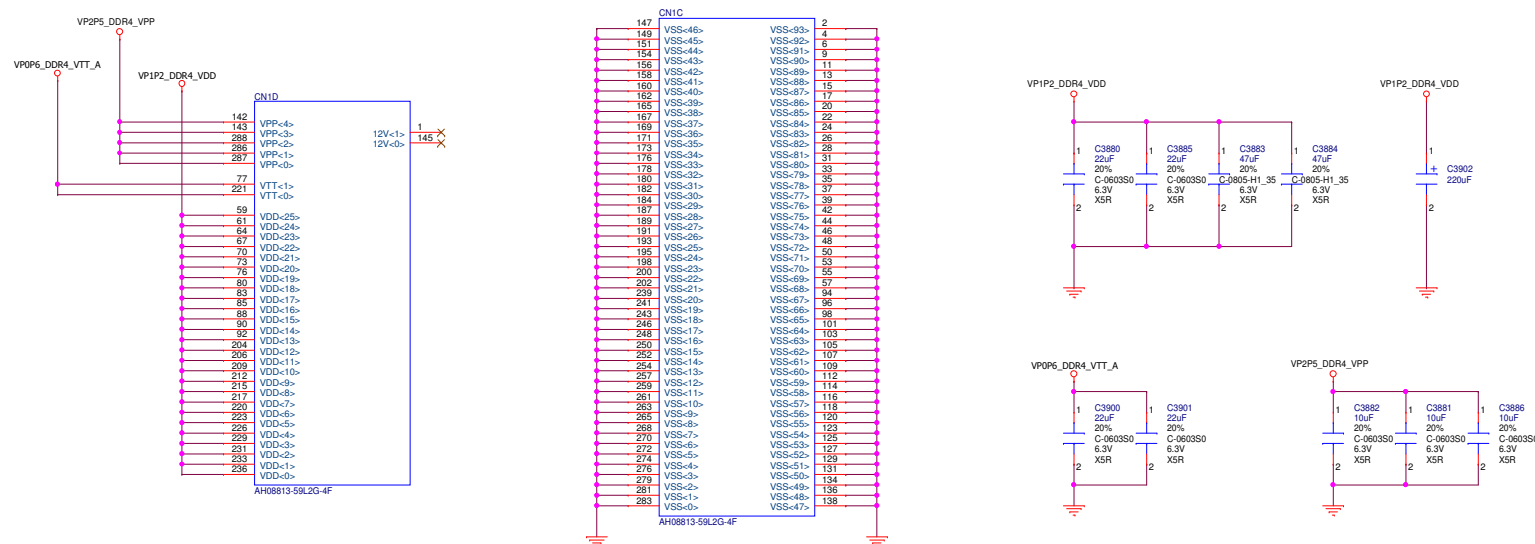
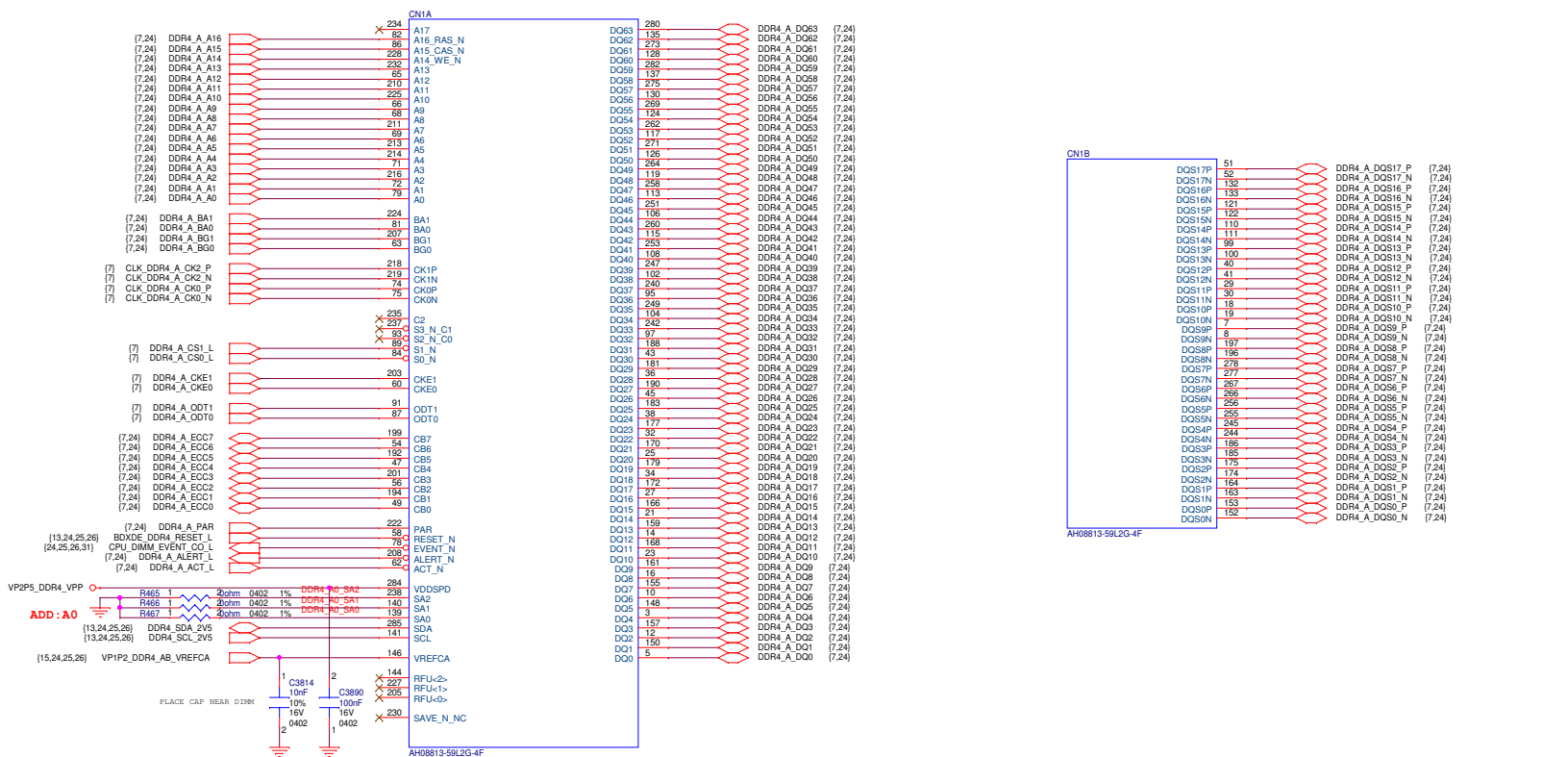




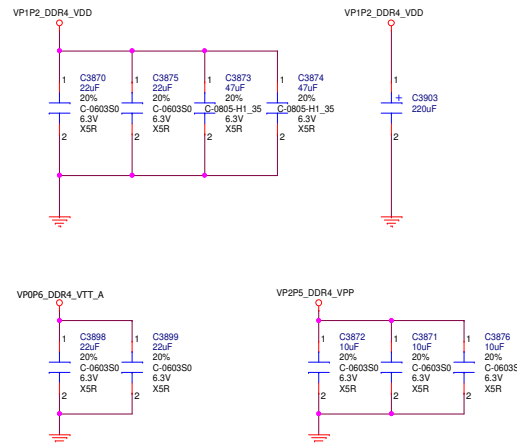
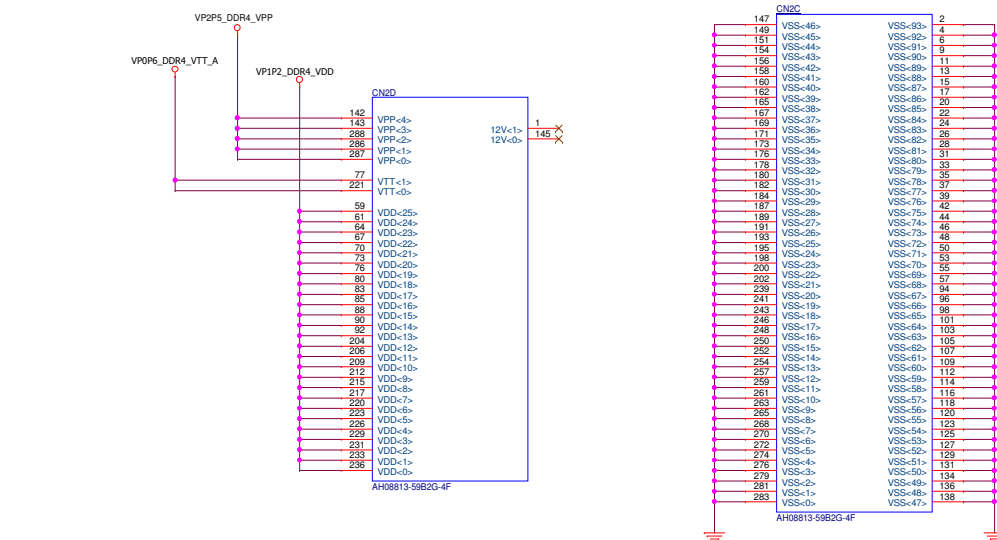
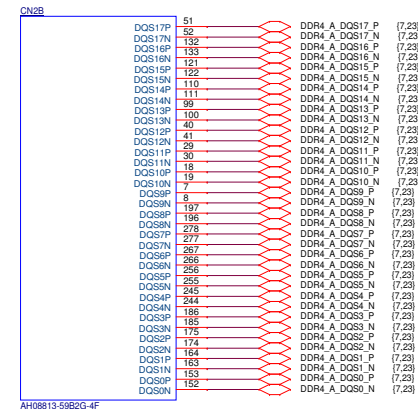
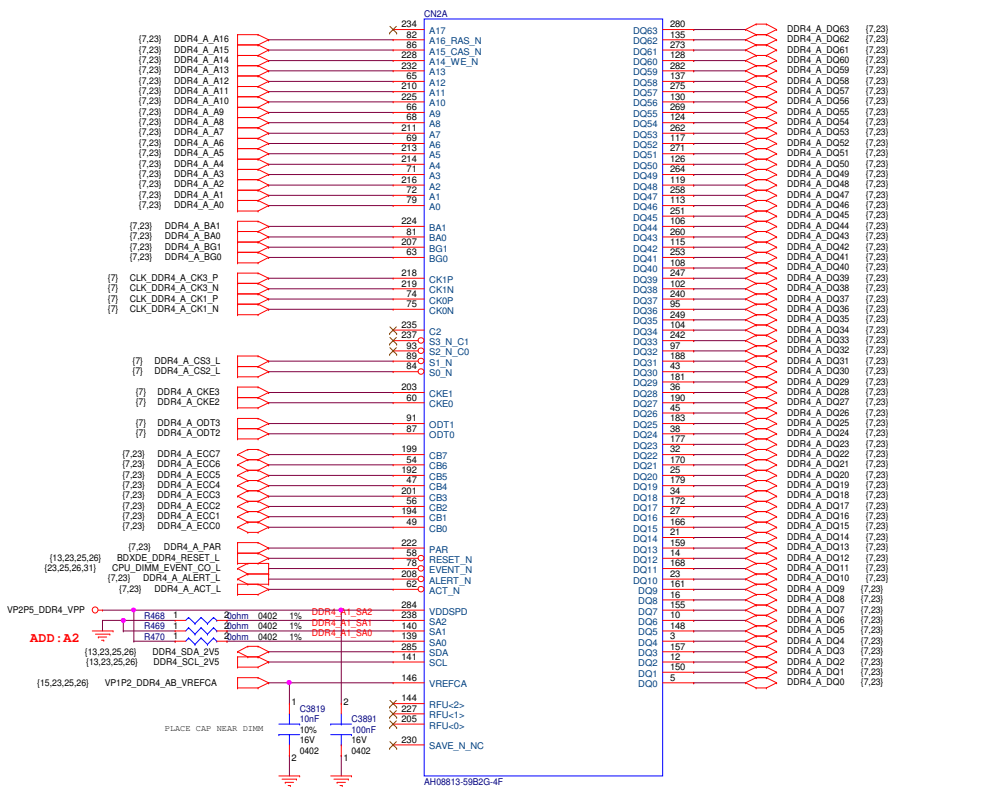




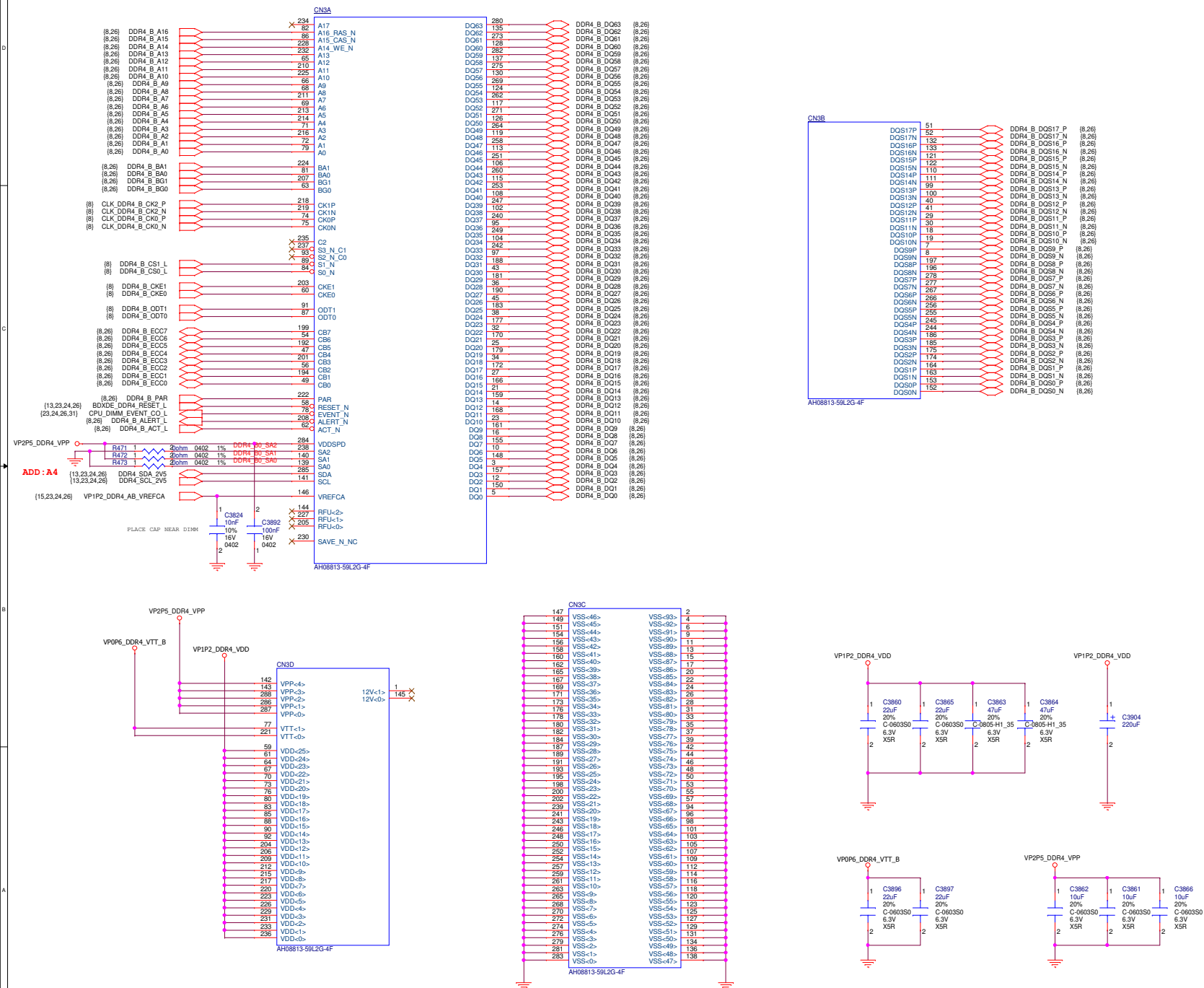
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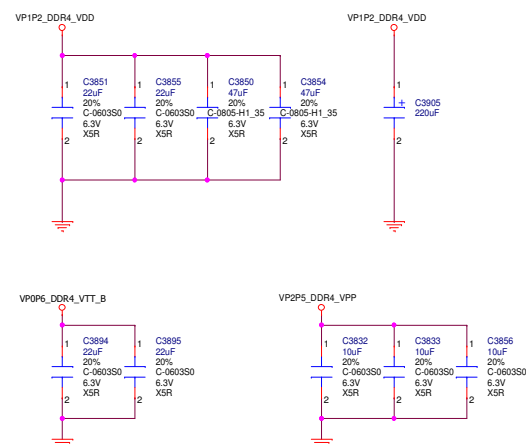
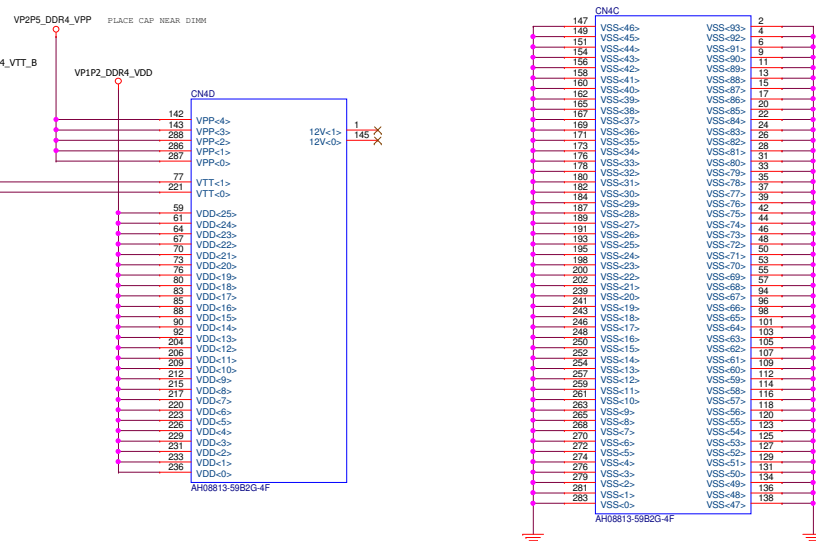
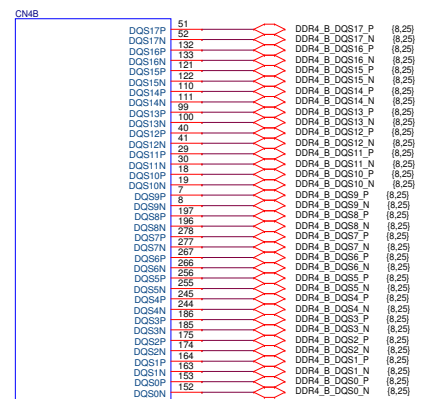
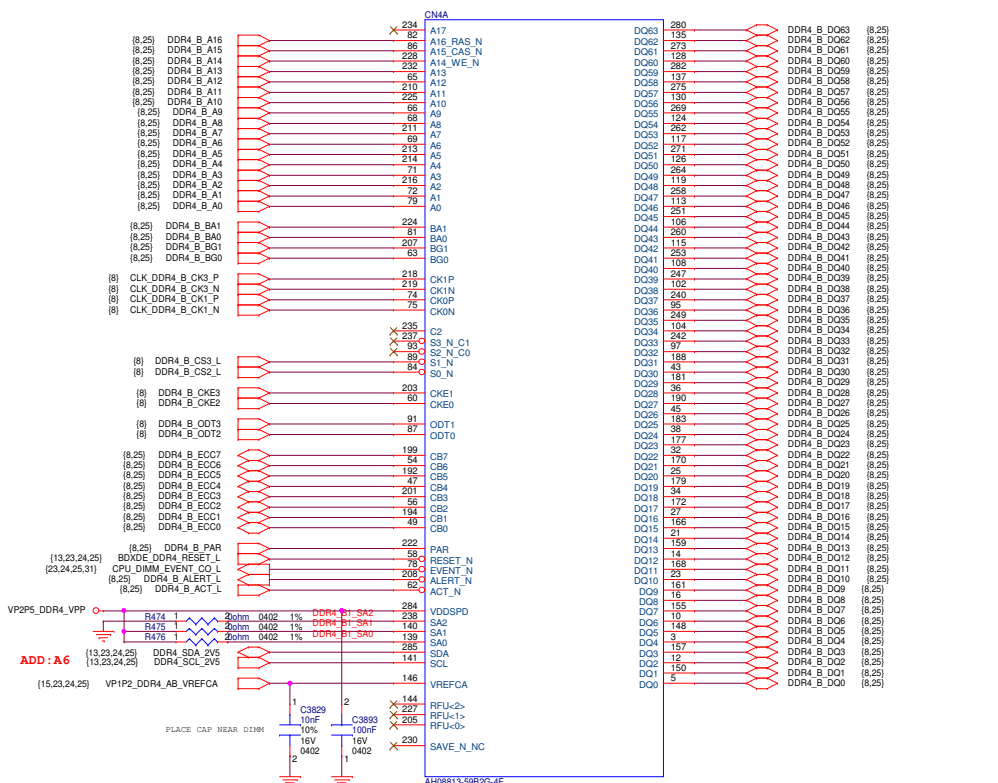
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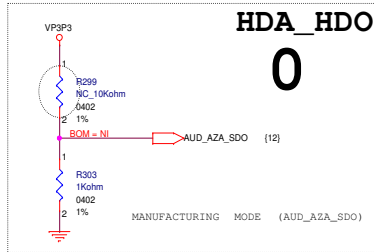
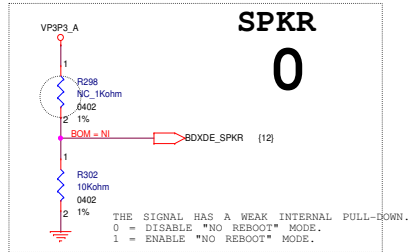
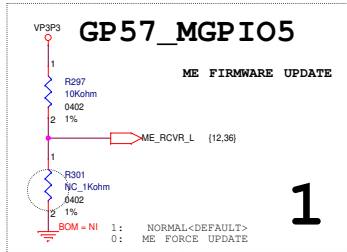
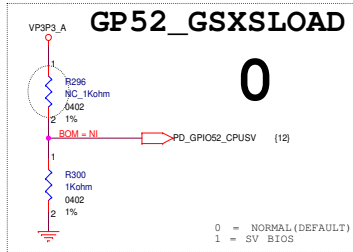
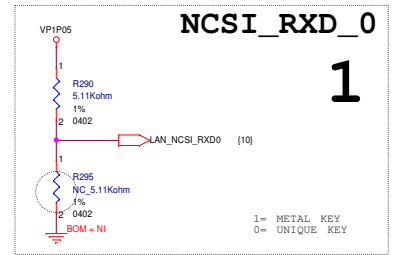
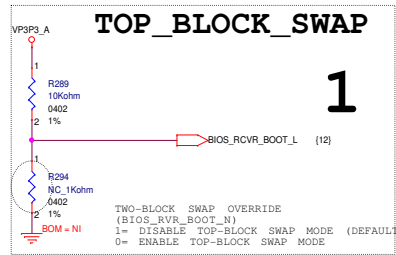
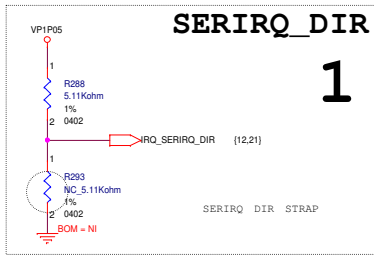
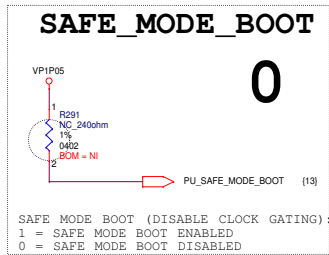
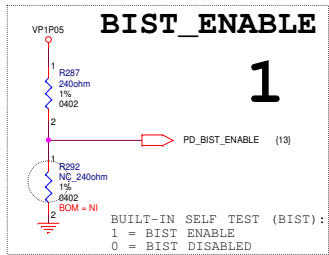


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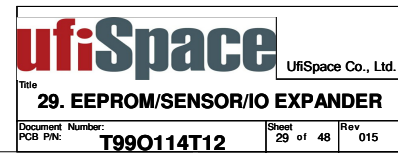
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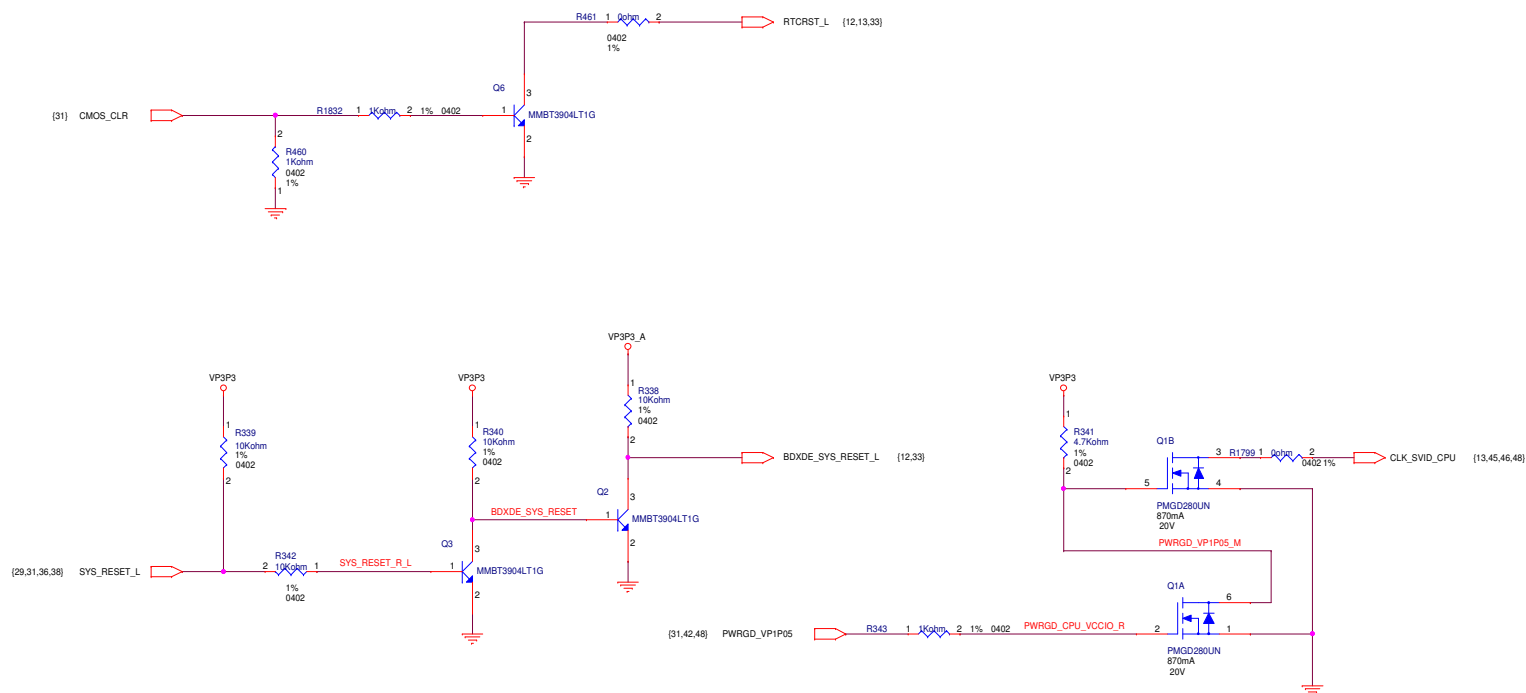


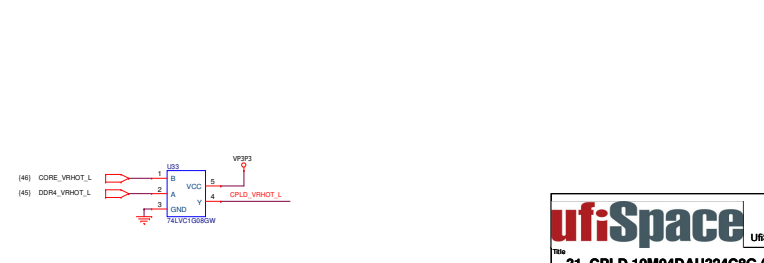
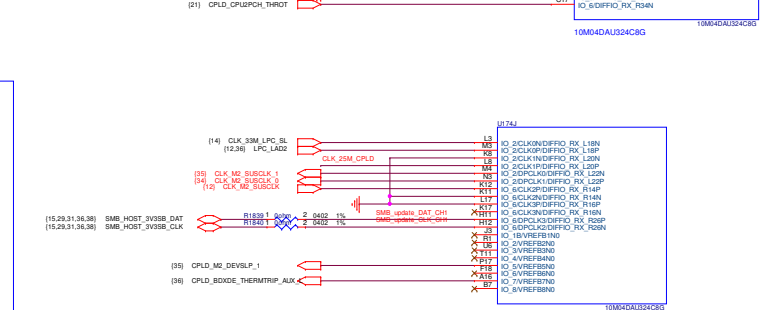
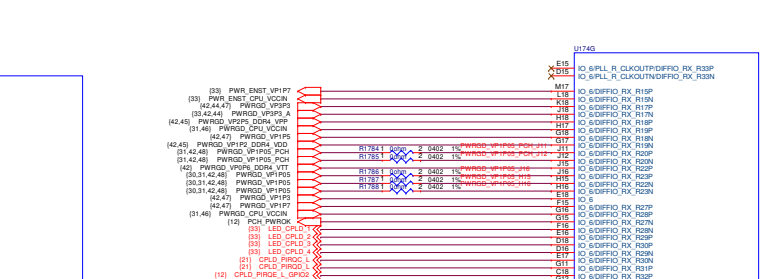
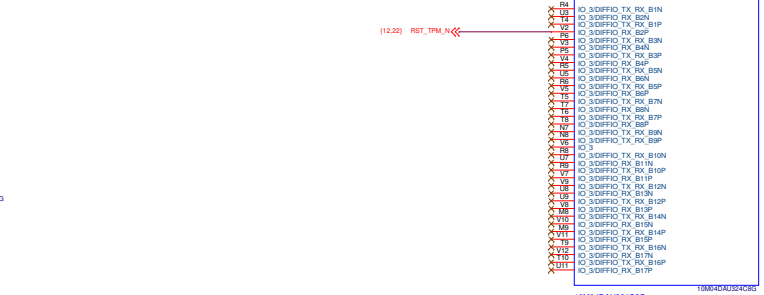


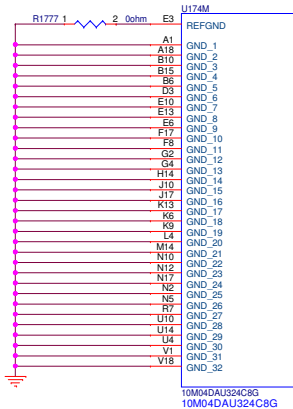
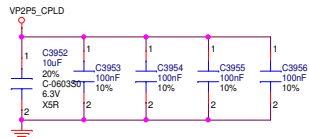
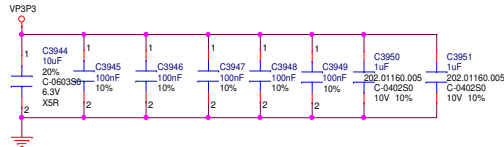
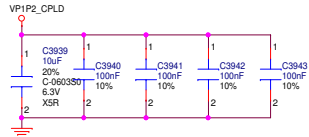
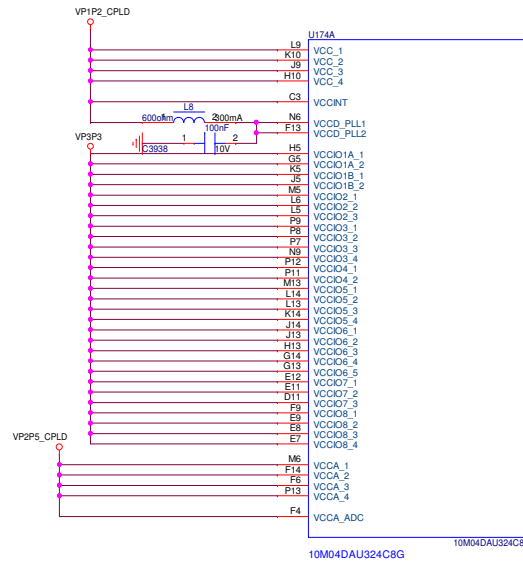
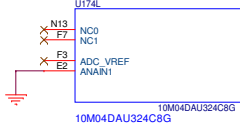
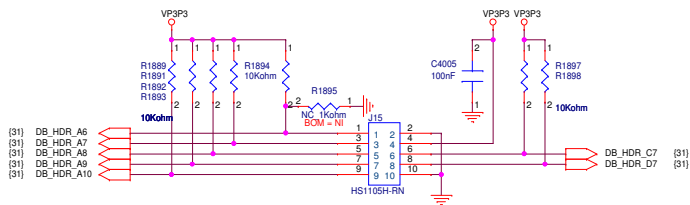
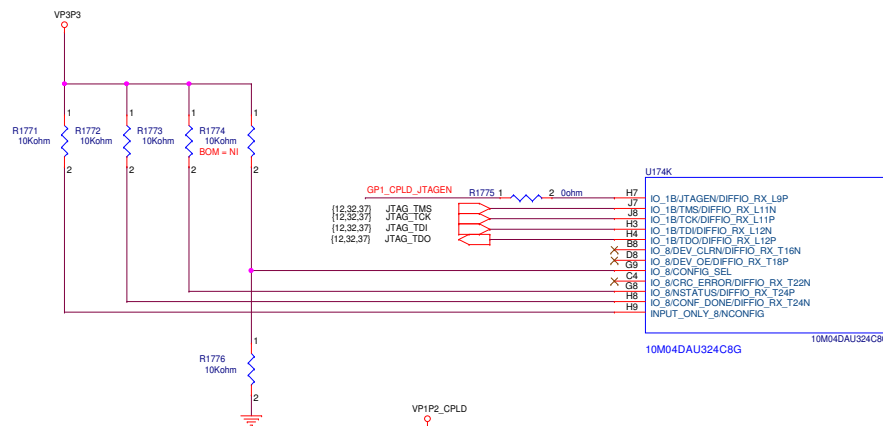
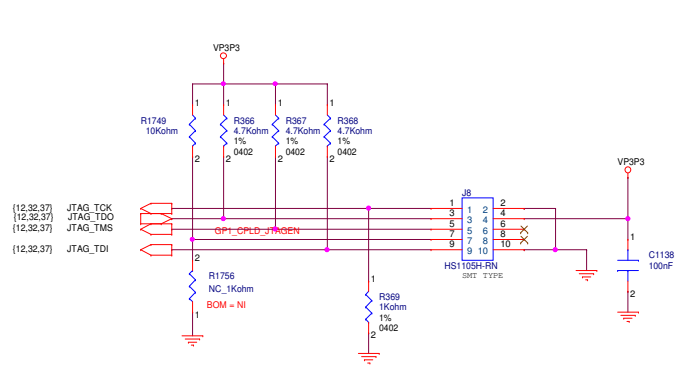
STRAP NAME	DEFAULT	DESCRIPTION
BOOT BIOS STRAPS (GP19, GP51)	1,1	BOOT BIOS DESTINATION 0 1 RESERVED 1 0 RESERVED 1 1 SPI (DEFAULT) 0 0 LPC
DMI_TERMINATION	0	DMI TX TERMINATION WHEN DCCOUPLED MODE. 0 = DMI TX IS TERMINATED TO VSS. 1 = DMI TX IS TERMINATED TO VCC/2.
BIOS_ADV_FUNCTIONS	0	DMI RX TERMINATION WHEN AC-COUPLED MODE: 0 = DMI RX IS TERMINATED TO VSS (DEFAULT) 1 = DMI RX IS TERMINATED TO VCC/2.
GSXDIN	0	DMI AC OR DC COUPLING? 0 = DMI IS IN AC-COUPLING MODE (SERVER/WORKSTATION ONLY, NOT MEANT FOR DESKTOP/MOBILE) 1 = DMI IS IN DC-COUPLING MODE (DESKTOP, MOBILE OR SERVER/WORKSTATION).
ADR_TRIGGER	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
SUSCLK	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
NCSI_TRI_EN CPU2PCH_THROT SPARE[0]	0,0,0	STRAPS HERE TO IDENTIFY WHICH SOCKET IS WHICH IN ORDER FOR PECI TO WORK
SPARE[1]	0	THIS IS THE DISABLE TO THE SC PCU RESET FSM 0 = PMC PSB BRINGS UP SOUTH COMPLEX 1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC
SPARE[2]	0	BYPASSES THE CRYSTAL CLOCK TO THE SCPLL 0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEFAULT) 1 = FORCES THE TEST CLOCK FROM TSTCLK_SC PINS
SPARE[3]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NO TEST CLOCK OVERRIDE (DEFAULT) 1 = TEST CLOCK OVERRIDE
SPARE[4]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NORMAL REFERENCE CLOCK PATH WITH CR BASED REFERENCE CLOCK SELECTION (DEFAULT) 1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS
UART_TXD[0]	0	JTAG PORT FOR NORTH COMPLEX TAP 0 = GB#_SDP# PINS ARE USED AS FUNCTIONAL PIN OR CAN BE USED FOR SC TAPS THROUGH TAP PROGRAMMING. (DEFAULT) 1 = PINS ARE USED AS JTAG PORT FOR NC TAP
UART_TXD[1]	0	CONTROLS THE SECURITY ATTRIBUTES ON THE NVM - FOR PRE-PRODUCT ON USAGE 0 = DISABLES NVM SECURITY (DEFAULT) 1 = SECURITY ENABLED

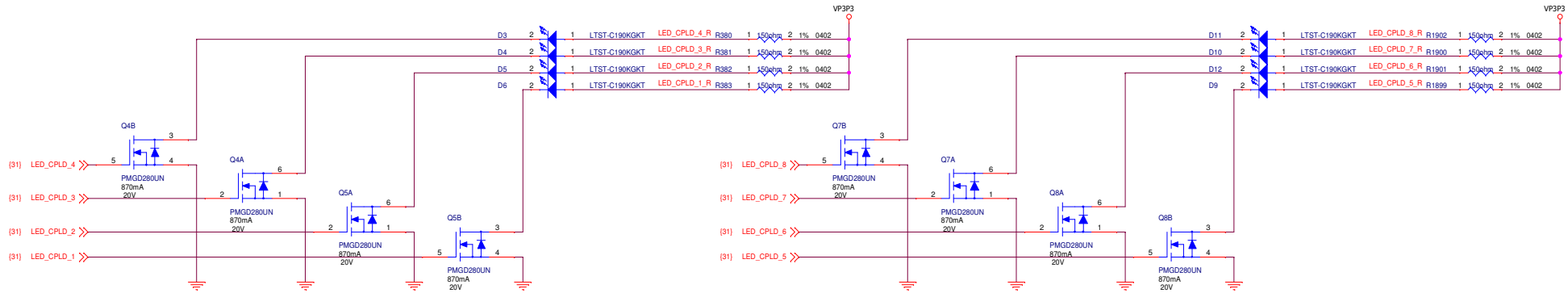
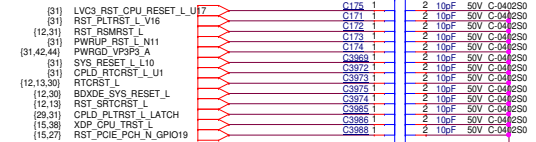
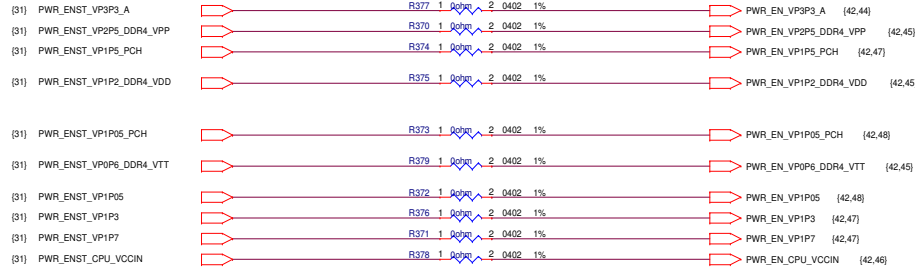
STRAP NAME	DEFAULT	DESCRIPTION
NCSI_ARB_OUT	1	USING COMBINED P1V05
DSWODVREN	1	0 = DISABLE INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR. THIS MODE IS ONLY SUPPORTED FOR TESTING ENVIRONMENTS. 1 = ENABLE DSW 3.3V-TO-1.05V INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR.
NCSI_RXD_1	0	ENABLE/DISABLE MANAGEABILITY TRAFFIC 0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT) 1 = LAN NOT AVAILABLE IN S5. MANAGEABILITY DISABLED.
INTVRMEN	1	INTEGRATED VRMS 0 = DCPSUS1, DCPSUS2 AND DCPSUS3 ARE POWERED FROM AN EXTERNAL POWER SOURCE. SERVERS SHOULD NOT PULL THE STRAP LOW. 1 = INTEGRATED VRMS ENABLED.
10GBE_MDIO_DIR_CTL_0 10GBE_MDIO_DIR_CTL_1	1,1	00 = BOTH LAN PORTS ARE DISABLED. 01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED. 10 = RESERVED 11 = BOTH PORT0 & 1 ARE ENABLED. (DEFAULT)
DDR3_4_STRAP	1	1 = DDR4 0 = DDR3
TXT_PLTEN	1	(INTEL? TXT) PLATFORM ENABLE STRAP. 0 = THE PLATFORM IS NOT INTEL TXT ENABLED. 1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED
TXT_AGENT	1	TXT AGENT (DRIVES TXT TRANSACTIONS): 1 = CPU IS TXT_AGENT 0 = CPU IS NOT TXT_AGENT
BIST_ENABLE	1	BUILT-IN SELF TEST (BIST): 1 = BIST ENABLED 0 = BIST DISABLED
SAFE_MODE_BOOT	0	SAFE MODE BOOT (DISABLE CLOCK GATING): 1 = SAFE MODE BOOT ENABLED 0 = SAFE MODE BOOT DISABLED



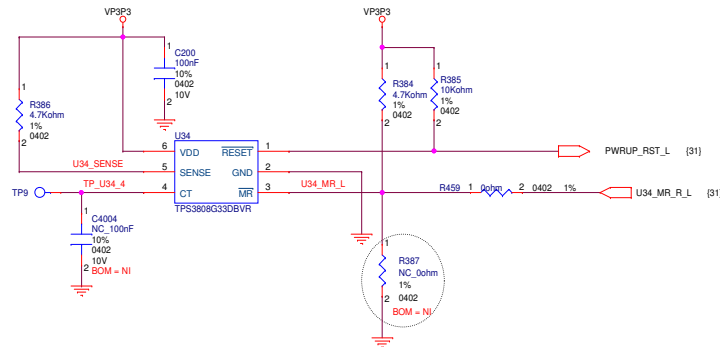




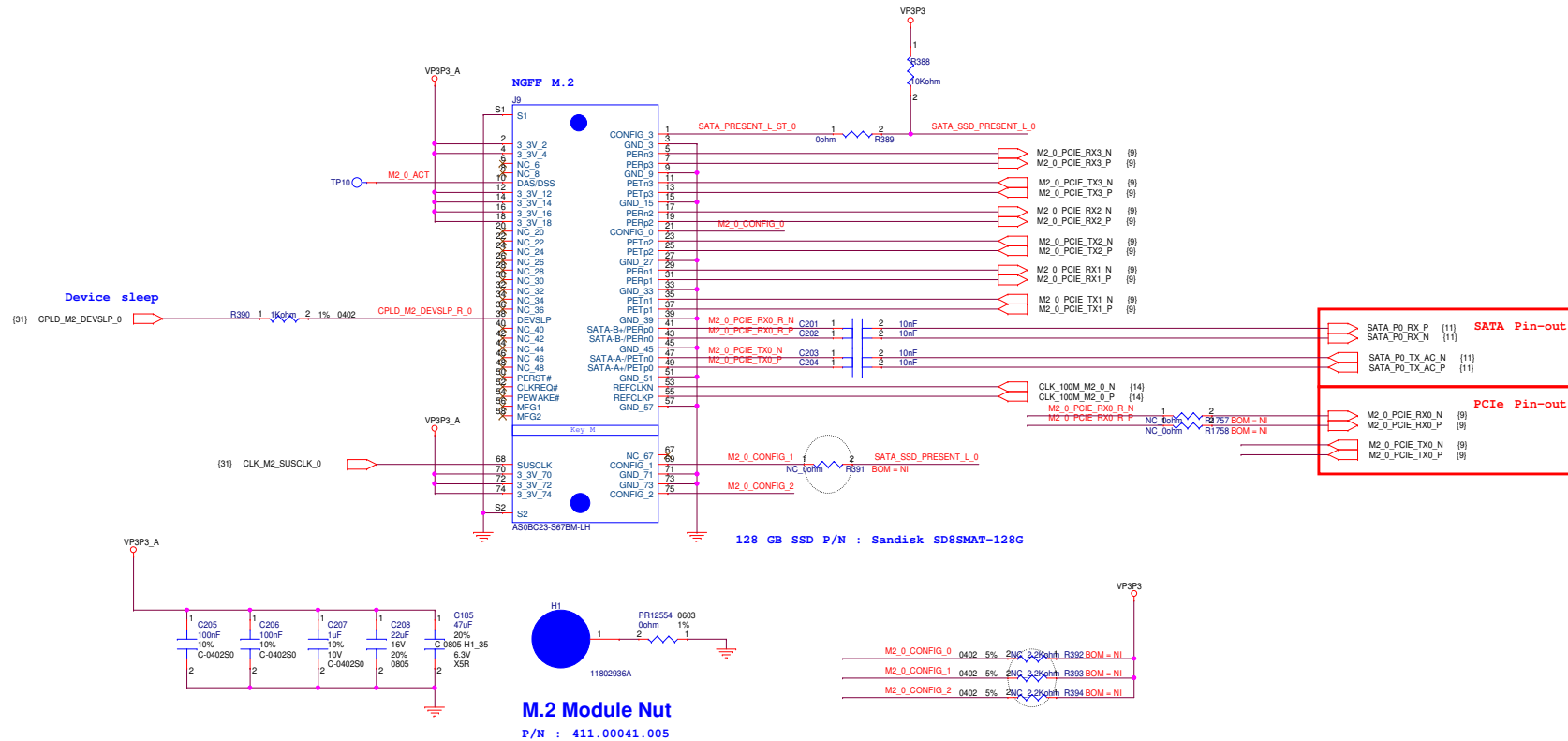




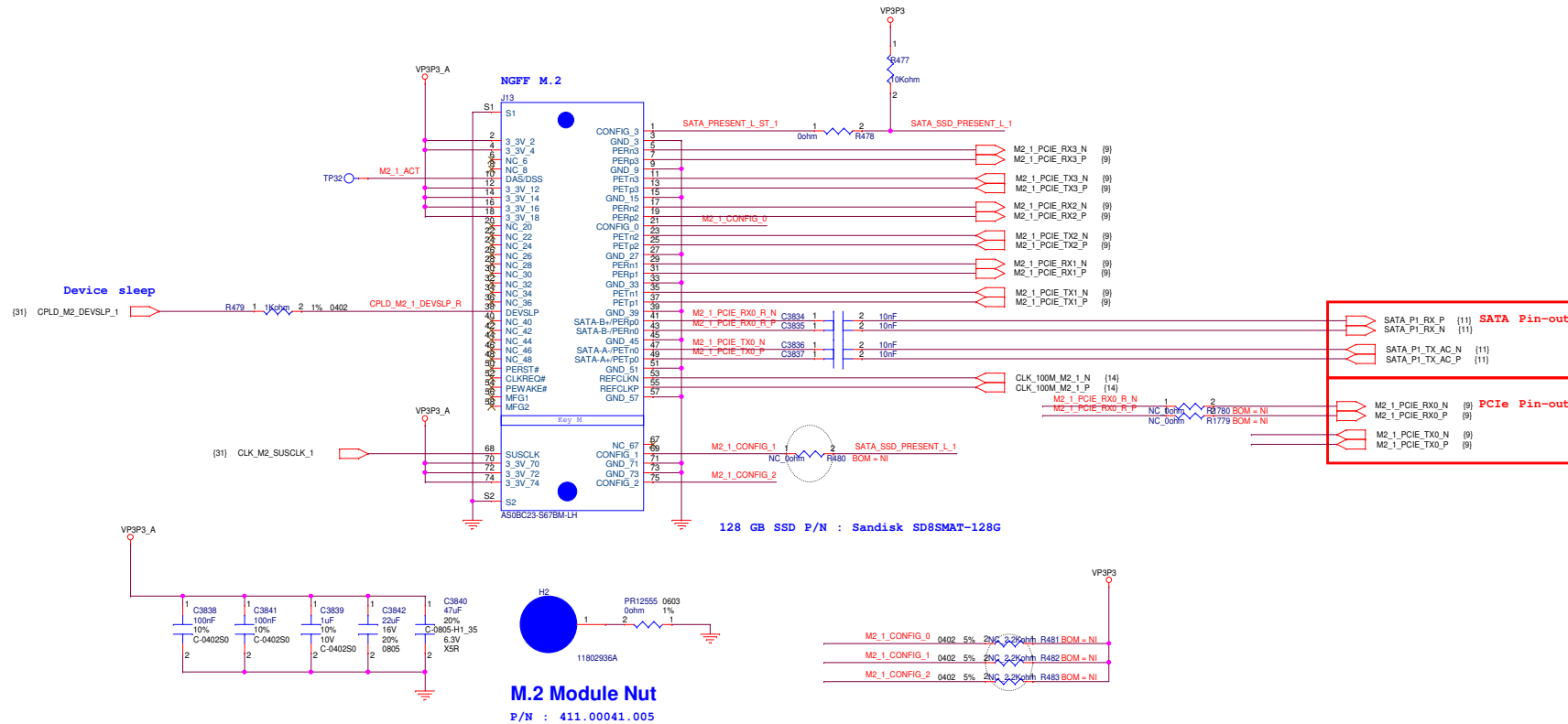
CPLD RESET IC



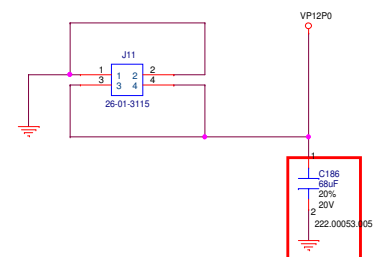
M.2_0 PCIe SATA Co-lay



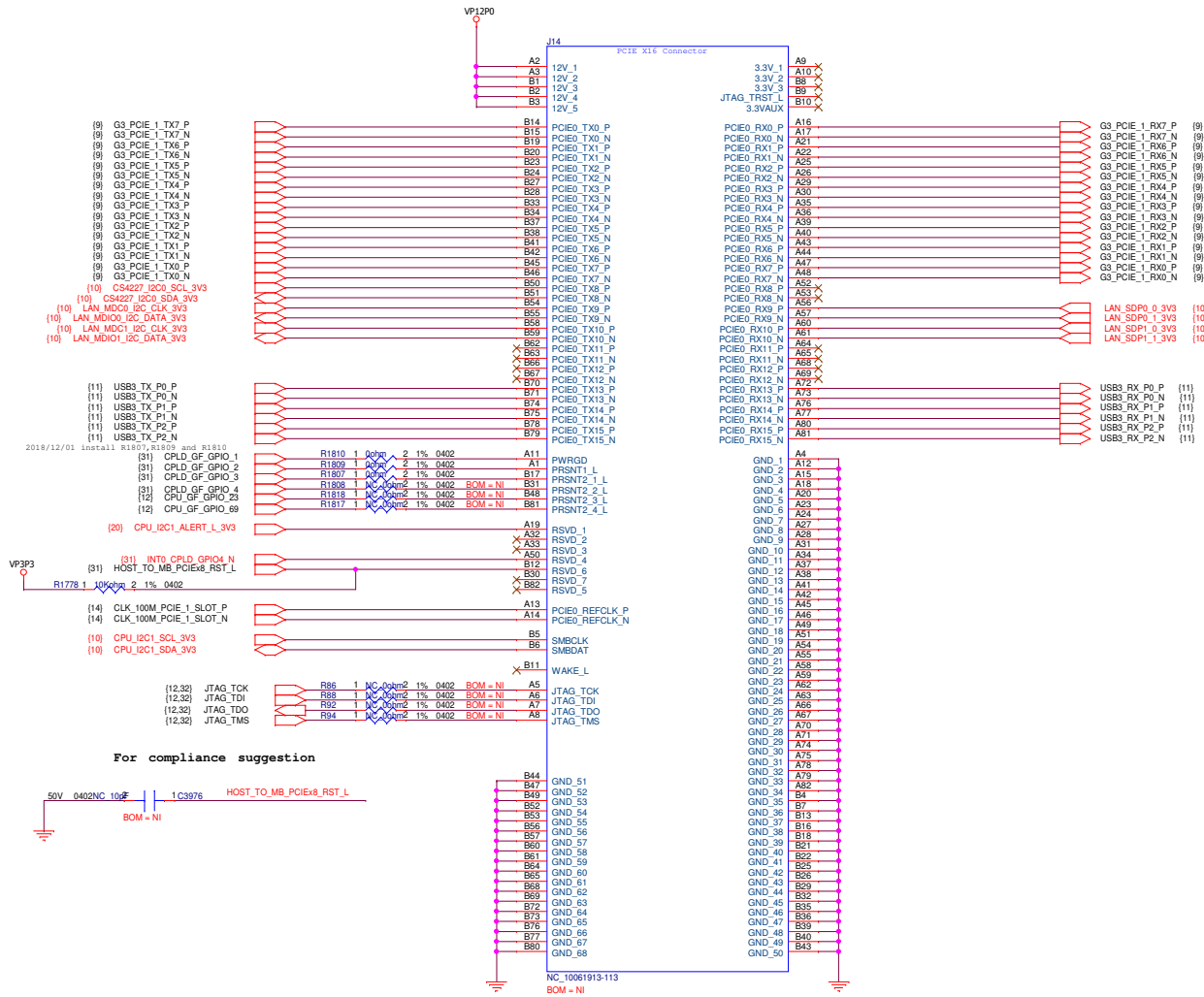
M.2_1 PCIe SATA Co-lay

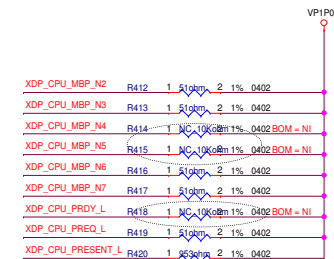
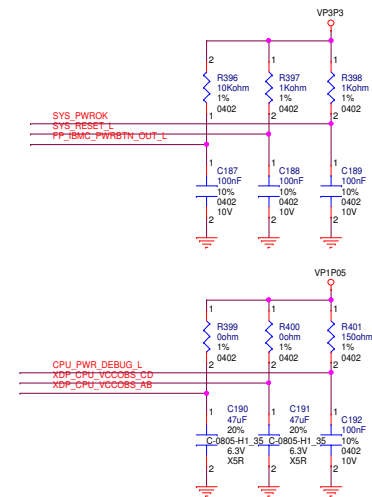
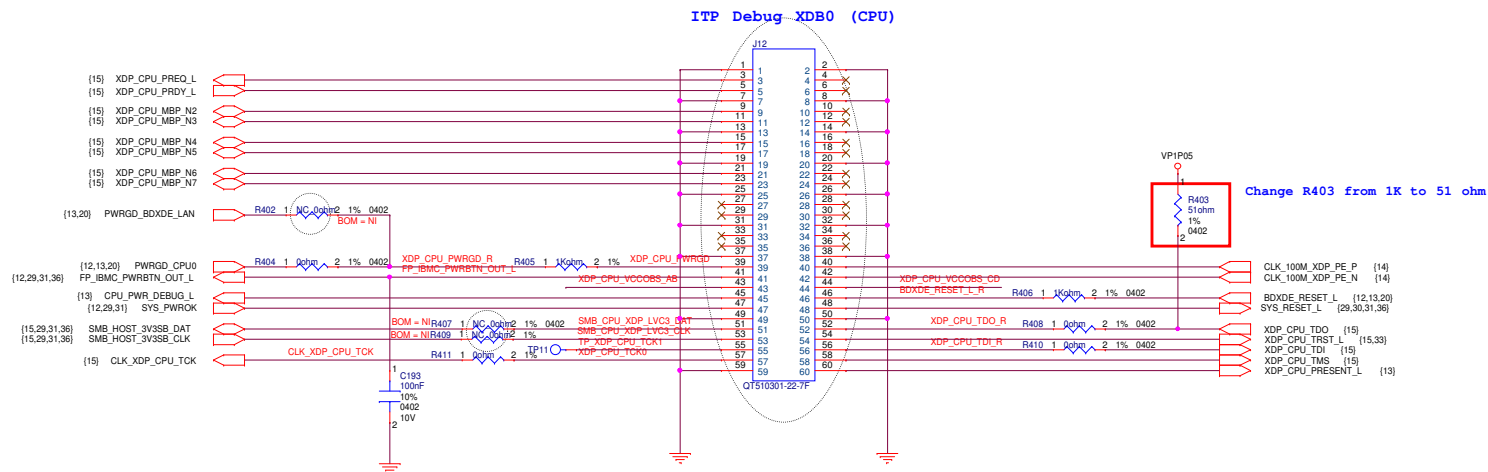


50V 0.0402NC 10µF 1C3977 BOM = NI HOST_TO_MB_BMC_RST_L
 50V 0.0402NC 10µF 1C3978 BOM = NI CPLD_PCIE_RESET_L
 50V 0.0402NC 10µF 1C3979 BOM = NI HOST_TO_MB_PCIE_X_RST_L
 50V 0.0402NC 10µF 1C3980 BOM = NI HOST_TO_MB_I2C_RST



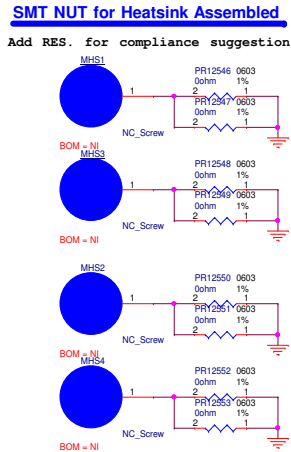
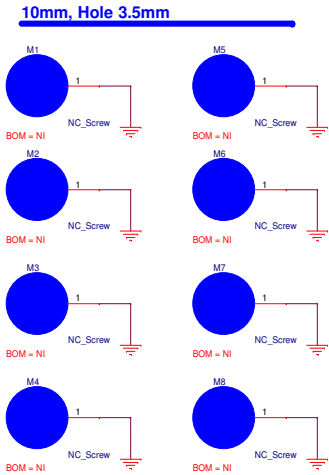
Gold Finger Connector





PLACE ALL THE CAPACITORS CLOSE TO THE XDP PIN.
FOR THE COUPLES OF LINES WITH DOUBLE CAPACITOR, ADD ONE PER XDP CONNECTOR

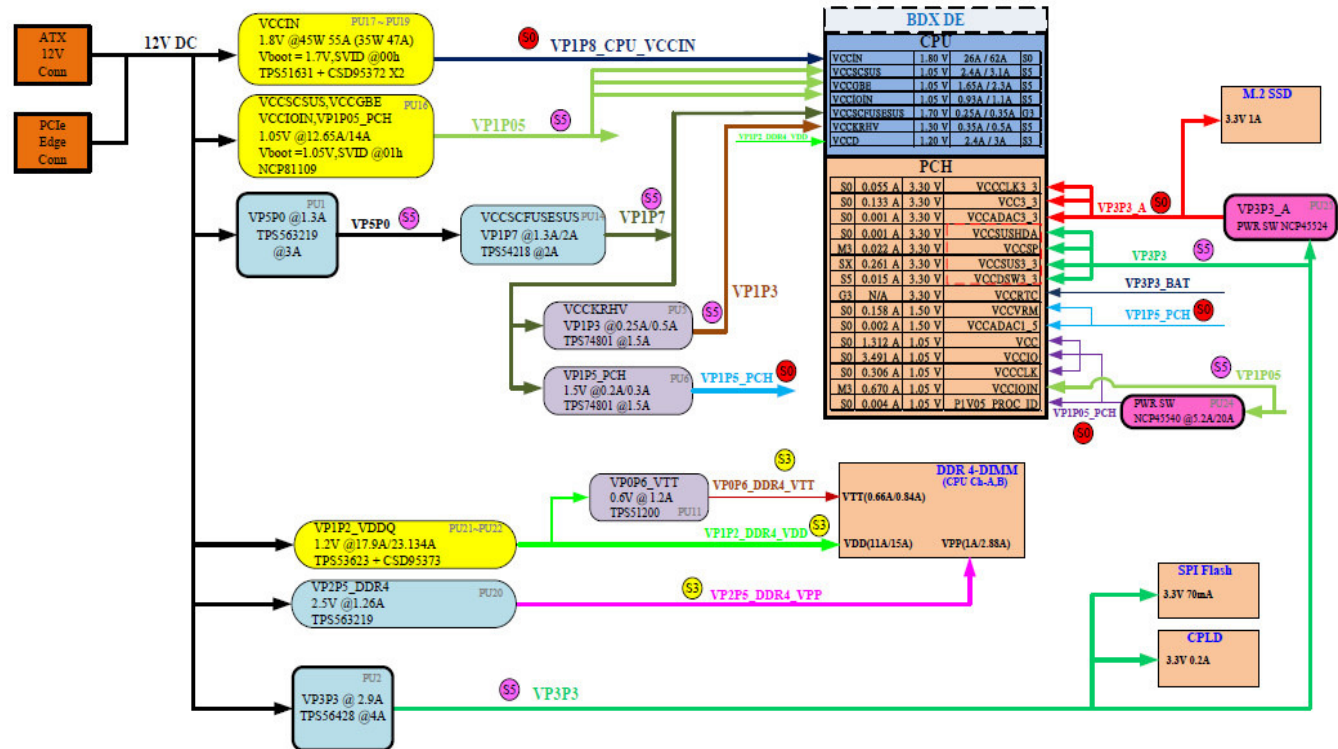
BOM ONLY PARTS



P/N: 400.00850.005
HEAT SINK CPU
HS4

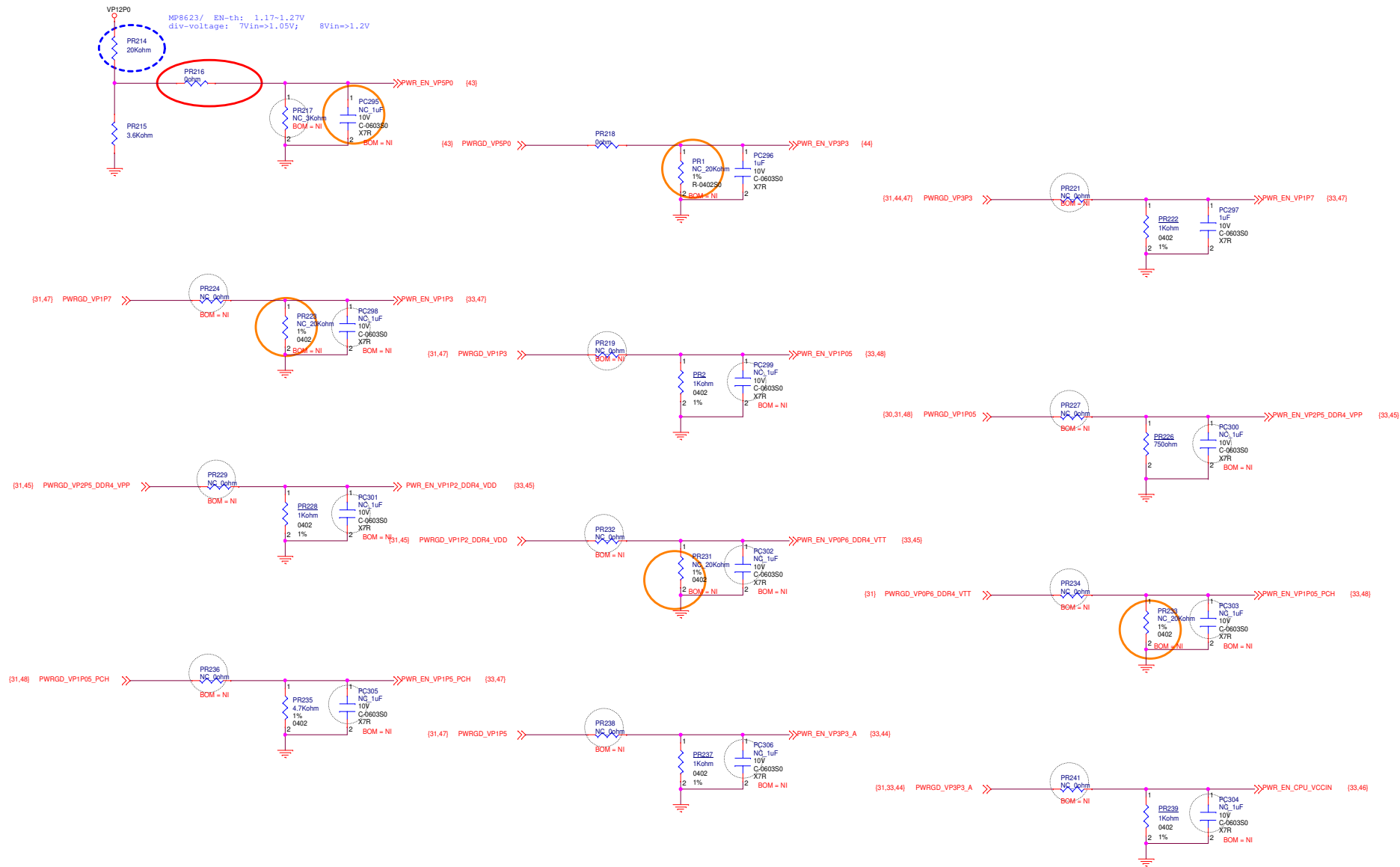
P/N: 309.00160.025
PCB
PCB1

2018/12/12 add PCB symbol

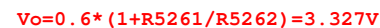


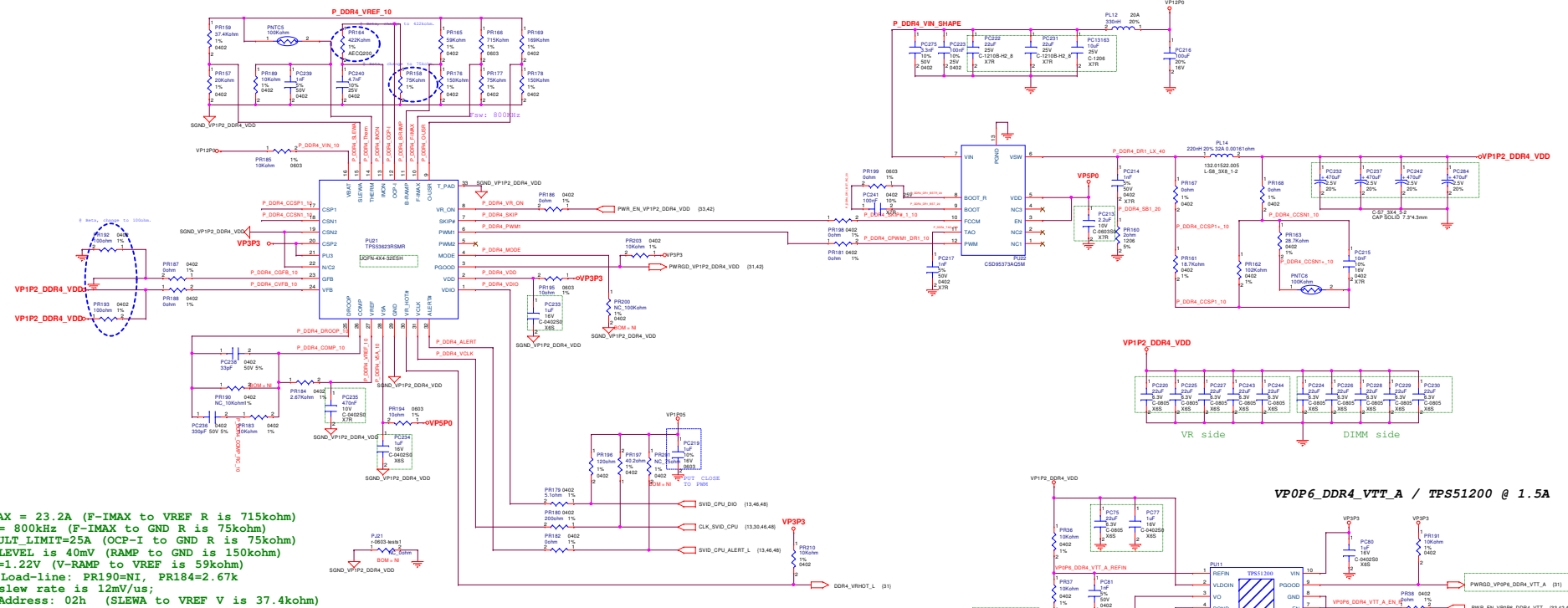
INDEX	FUNCTION	MAX AMPS	LABEL	BASED ON	PAGE	INPUT
1	CPU_VCCIN_1.8V	55	VP1P8_CPU_VCCIN	TPS51631ARSMR	46	VP12P0
2	CPU_1.05V	14	VP1P05	TPS53623RSMR	48	VP12P0
3	CPU_1.7V	2	VP1P7	TPS54218RTER	47	VP5P0
4	CPU_1.3V	0.5	VP1P3	TPS74801DRCR	47	VP1P7
5	CPU_PCH_1.05V	5.2	VP1P05_PCH	NCP45540IMNTWG-H	48	VP1P05
6	CPU_PCH_1.5V	0.162	VP1P5_PCH	TPS74801DRCR	47	VP1P7
7	DDR4_1.2V	24.45	VP1P2_DDR4_VDD	TPS53623RSMR	45	VP12P0
8	DDR4_0.6V	1.2	VP0P6_DDR4_VTT	TPS51200DRCT	45	VP1P2_DDR4_VDD
9	DDR4_2.5V	2.4	VP2P5_DDR4_VPP	MPQ8623GD-Z	45	VP12P0
10	5.0V STBY	1.3	VP5P0	MPQ8623GD-Z	43	VP12P0
11	3.3V STBY	6.22	VP3P3	MPQ8633AGL-Z	44	VP12P0
12	3.3V	4.5	VP3P3A	NCP45540IMNTWG-H	44	VP3P3
13	CPLD_1.2V	0.083	VP1P2_CPLD	TPS74801DRCR	47	VP3P3
14	CPLD_2.5V	0.024	VP2P5_CPLD	TPS74801DRCR	47	VP3P3

Power up Sequence



layout placement refer to "T770925T00_025_20180328d"

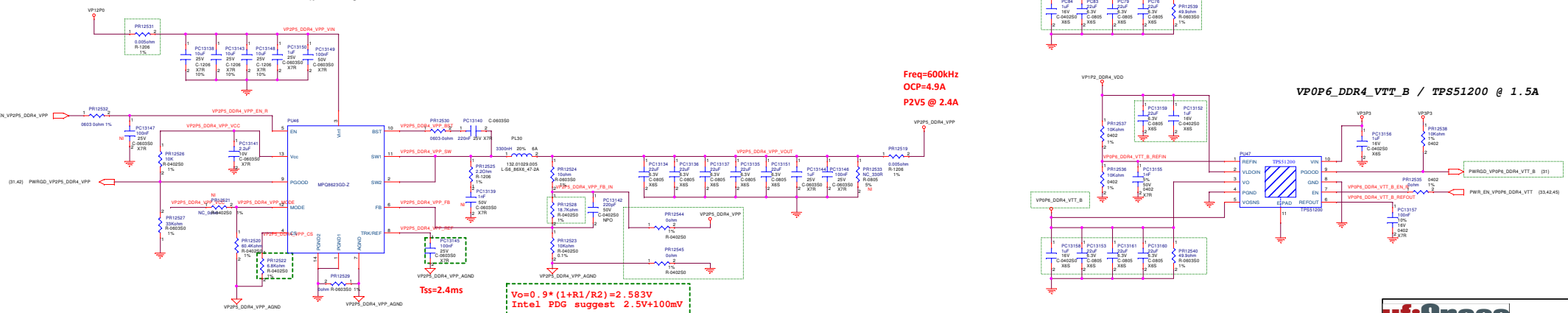




- ```

1. ICC_MAX = 23.2A (F-IMAX to VREF R is 715kohm)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=25A (OCP-I to GND R is 75kohm)
4. RAMP_LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.22V (V-RAMP to VREF is 59kohm)
6. Zero Load-line: PR190=NI, PR184=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 02h (SLEWA to VREF V is 37.4kohm)

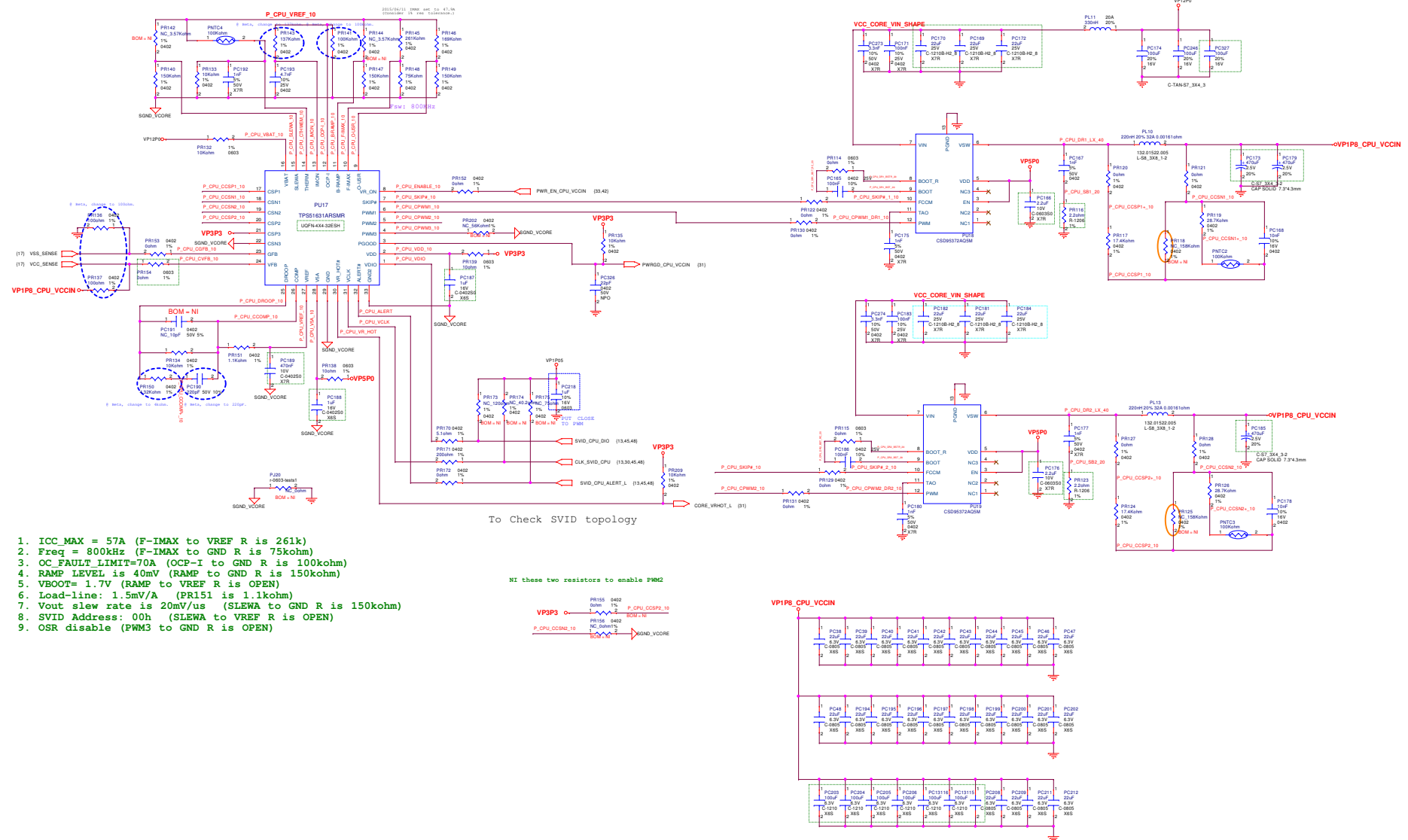
```

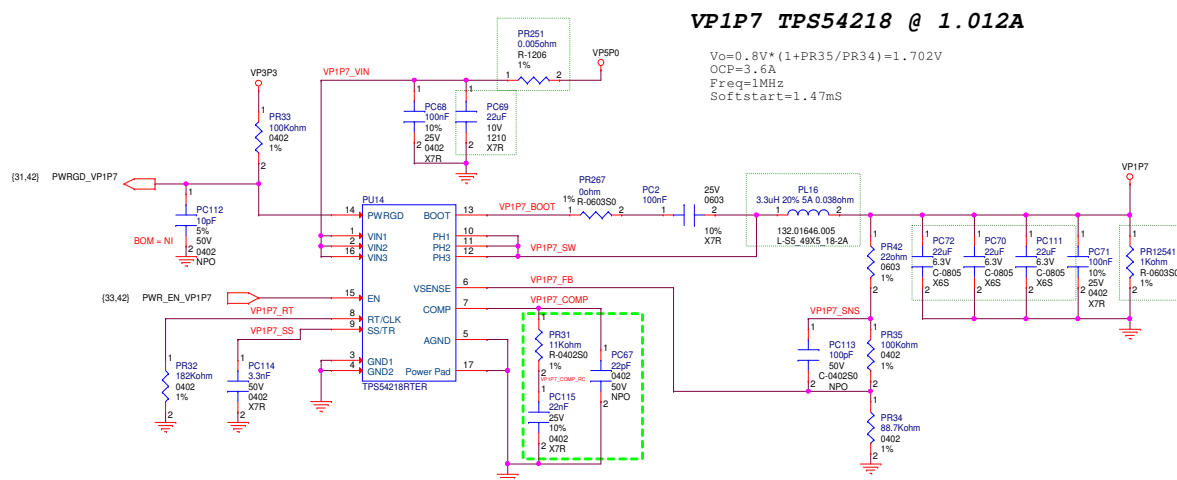
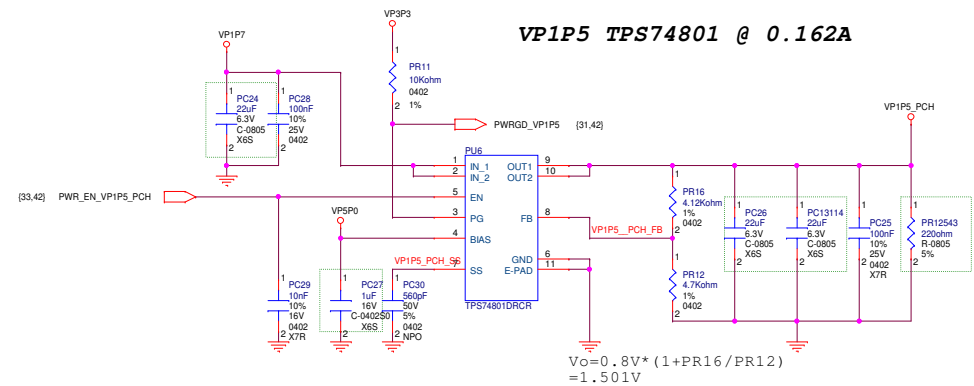
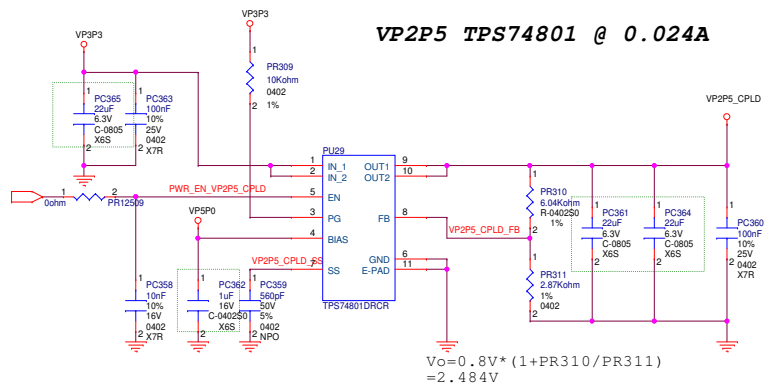
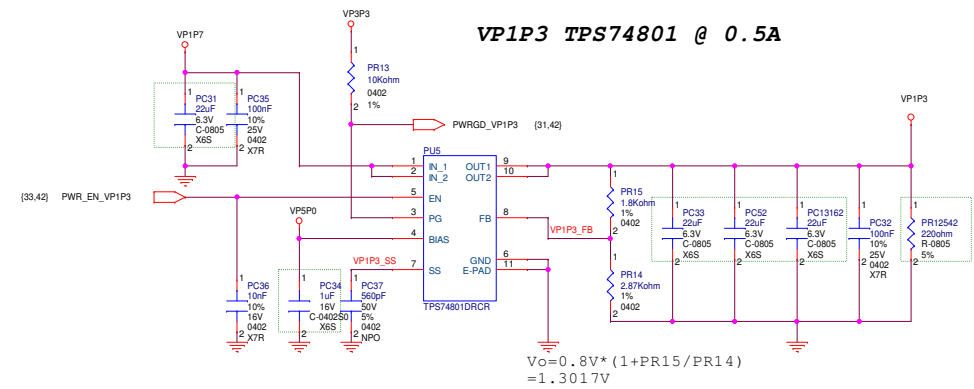
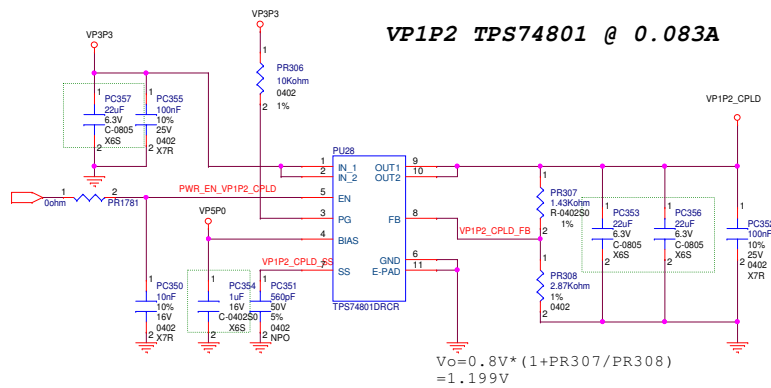


Freq=600kHz  
OCP=4.9A  
P2V5 @ 2.4A

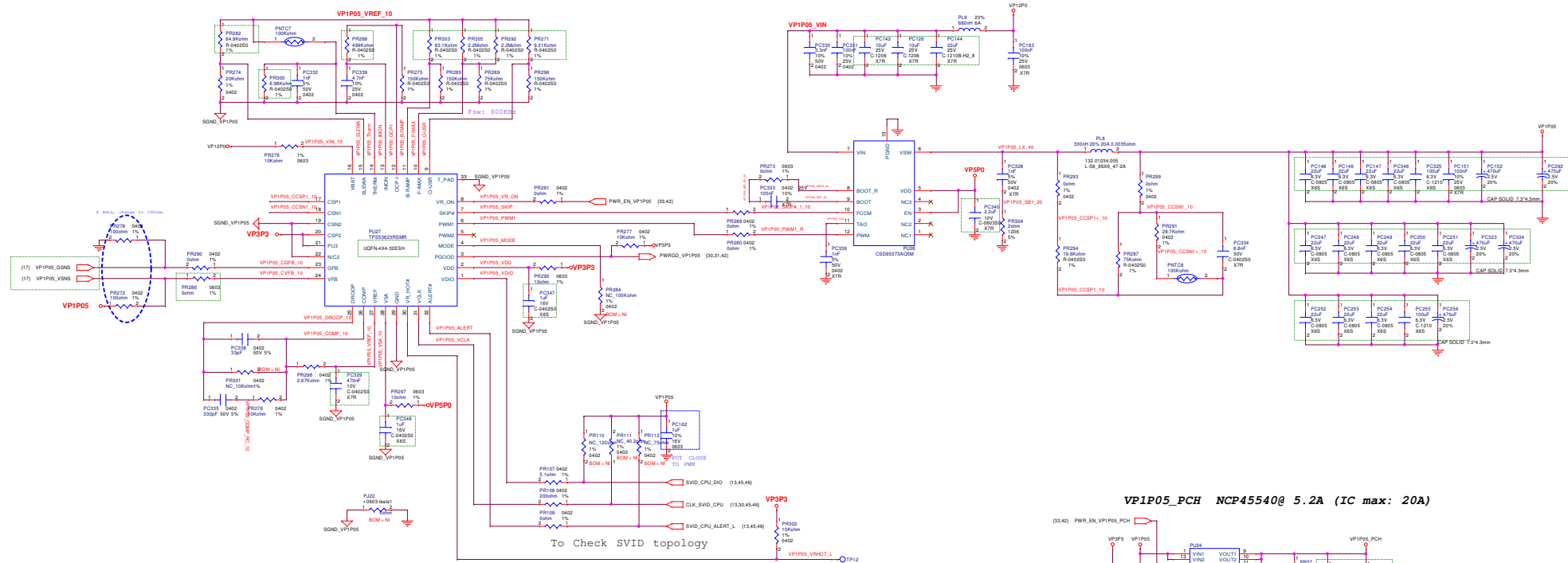
VP0P6\_DDR4\_VTT\_B / TPS51200 @ 1.5A

```
VCC_Core TPS51631A @ 25W 34Amax (15A TDC)
 35W 47Amax (21A TDC, OCP set to 65A)
 45W 55Amax (26A TDC)
```





## VP1P05\_Combined @ 14Amax (12.65A TDC)



- ```

1. ICC_MAX = 15.2A (F-IMAX to VREF R is 1100k)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=20A (OCP-I to GND R is 150kohm)
4. RAMP_LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.049V (V-RAMP to VREF is 93.1kohm)
6. Zero Load-line: PR301=NI, PR298=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 01h (SLEWA to VREF V is 64.9kohm)

```

